

# Memory Configurator

Lenovo ThinkStation P5



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## Overview

The purpose of this document is to provide high-level guidance for users to be able to identify the memory components of the system as well as optimally configure their system memory in the ThinkStation P5 platform to yield best performance.

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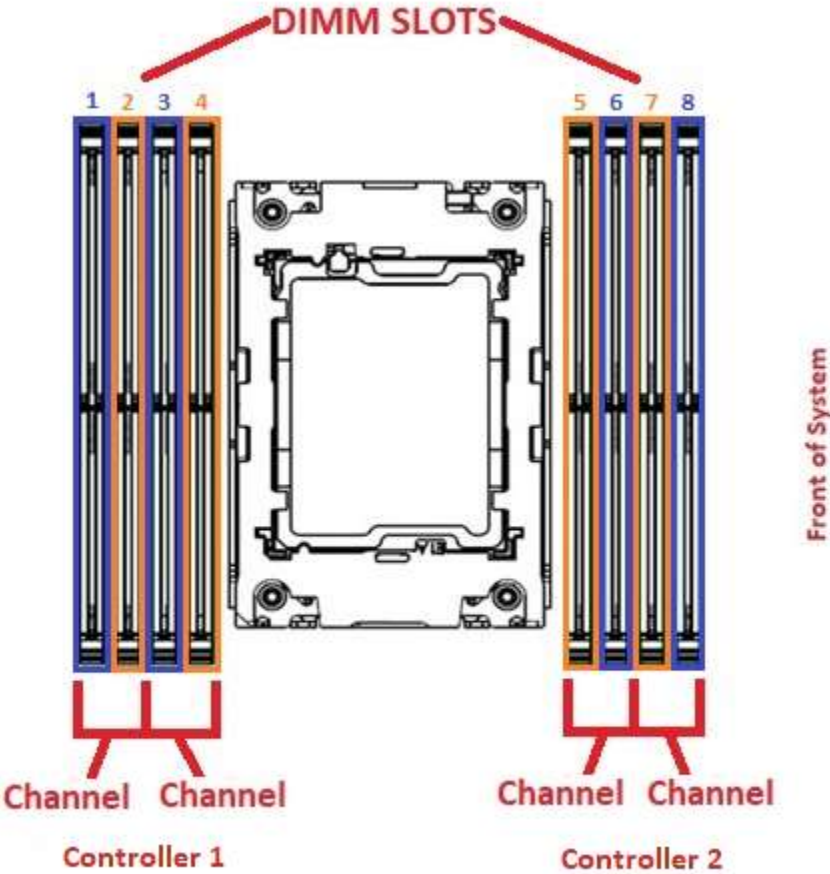
## Section 1 – Platform Memory Architecture

The launch of the latest Intel platform introduces support for the DDR5 memory DIMMs. The P5 system offers eight DIMM slots with quad channel architecture. DDR5 memory offers a variety of key design features. The most obvious of these features is that when utilizing the right processor and memory combination, the system has the ability to reach higher memory bandwidth speeds than the previous generation. The P5 can reach speeds of up to 4800MHz when using the system in a single DIMM per channel (4 DIMMs) configuration with certain CPUs. The following sections detail how to reach the maximum speed available.

## Section 2 – P5 Memory Layout Visual

The below diagram in Figure 1 shows a high-level visual layout of the memory DIMM slots in the ThinkStation P5 platform. Slots 1-4 utilize memory controller 1 while slots 5-8 utilize memory controller 2. Each adjacent Blue and Orange DIMM slot make up a single channel. For example, slots 1 and 2 share a channel. Blue slots will be populated first. Additionally, See Section 4 for the Memory Fill Order.

Figure 1 – P5 Motherboard DIMM Layout with Slot, Channel, and Controller Identification



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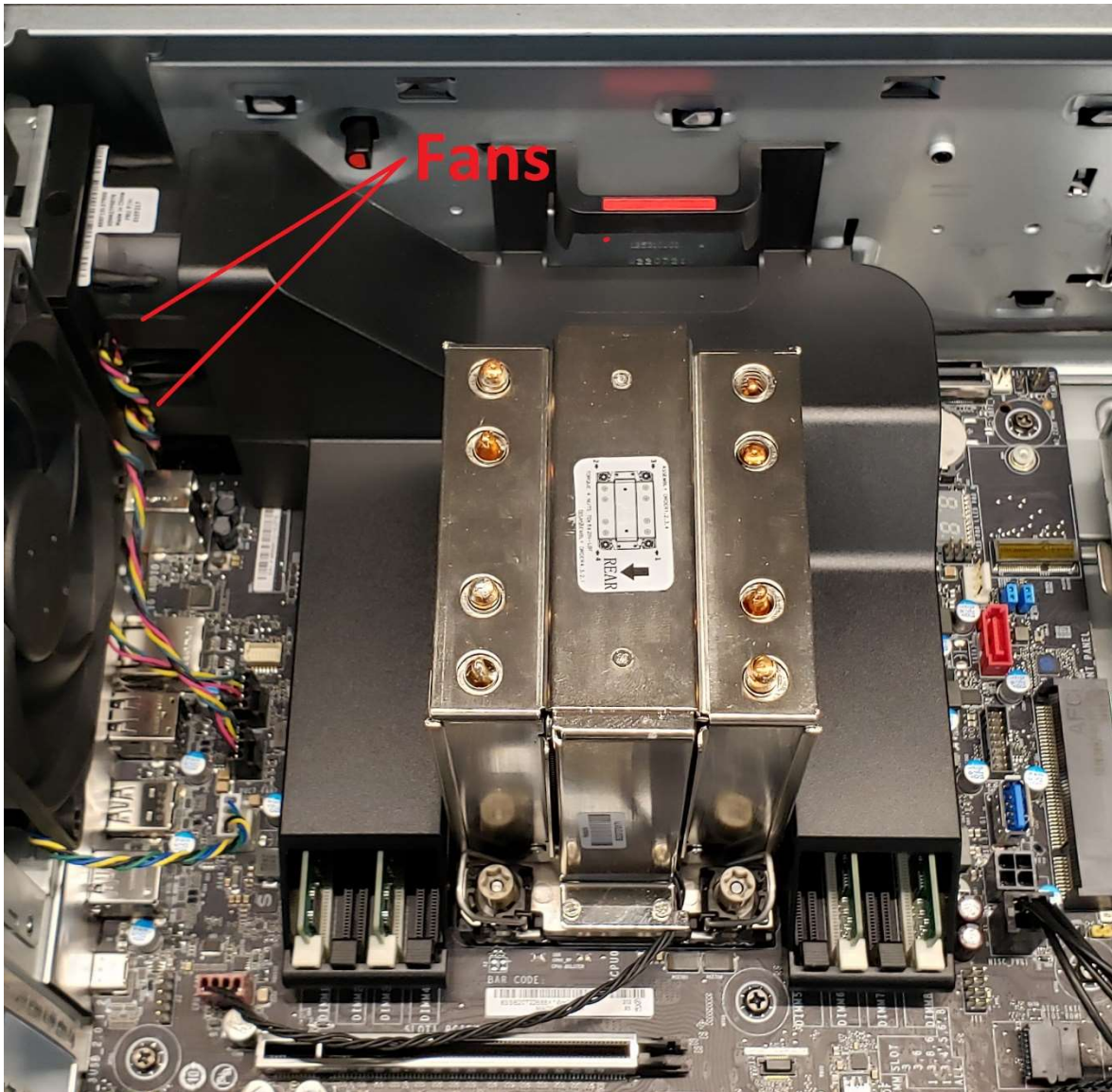
## Section 3 – P5 Memory Configurations

The ThinkStation P5 platform has 4-channels for 8 DIMM slots with a maximum of 512GB of system memory. The Lenovo ThinkStation P5 supports 16/32/64GB DDR5 RDIMMs for Intel 4th Gen Intel Xeon W-series Processors.

The following guidelines are recommended by Lenovo for obtaining the best memory bandwidth from the ThinkStation P5 platform.

- UDIMMs are not supported.
- DIMMs must be of the same type and capacity. DIMMs sharing a channel must be identical.
- Regardless of the number of DIMMs installed, there are two DIMM fans mounted to the rear of the system that use a DIMM slot cover to draw air over the DIMM slots and push the air out the rear of the system. See Figure 2 below for reference.
- When there are four or less DIMMs each DIMM has a dedicated channel, and the system is capable of running at a maximum speed of up to 4800MHz. If the system is utilizing 6 or 8 DIMMs, the system will run with 2 DIMMs per channel. When there are 2 DIMMs per channel the maximum memory speed of the system is reduced to 4400MHz.
- Maximum running speed is dependent on the processor used.

Figure 2 – P5 DIMM Slots Cover and Fans



# Section 4 – P5 Memory Fill Order

It is important to make sure the proper memory fill order is being utilized to get the best possible memory performance from the ThinkStation P5 workstation. Table 1 below shows the recommended fill order based on the number of DIMMs being used.

Table 1 – P5 DIMM Slot Fill Order Recommendations

Quantity of DIMMs	DIMM Slot Installation Order	Maximum Speed
1 DIMM	DIMM Slot 3	Up to 4800MHz
2 DIMMs	DIMM Slots 3, 6	Up to 4800MHz
3 DIMMs	Not Supported <sup>1</sup>	
4 DIMMs	DIMM Slots 1, 3, 6, 8	Up to 4800MHz
5 DIMMs	Not Supported <sup>1</sup>	
6 DIMMs	DIMM Slots 1, 3, 4, 5, 6, 8	Up to 4400MHz <sup>2</sup>
7 DIMMs	Not Supported <sup>1</sup>	
8 DIMMs	DIMM Slots 1 – 8 (Fully Populated)	Up to 4400MHz <sup>2</sup>

Note 1: Certain configurations with an odd total number of DIMMs can adversely affect performance and are therefore not supported.

Note 2: The P5 workstation is designed with 4 memory channels for the CPU. When there are 4 or less DIMMs properly installed in the system each DIMM has a dedicated channel, and the system is capable of running at a maximum speed of up to 4800MHz. Utilizing 6 or 8 DIMMs requires utilizing 2 DIMMs per channel. When there are 2 DIMMs per channel the memory runs at a maximum speed of up to 4400MHz. All maximum speeds are also dependent on the CPU being utilized.



# Revision History

Version	Date	Author	Changes/Updates
1.0	4/19/23	Scott C	Initial release