Overview

Overview of the Cisco Nexus 3550-T Switches

The Cisco Nexus 3550-T Programmable Switch Platform is a powerful top-of-rack Ethernet switch and application platform with a unique low-latency design. It offers comprehensive layer 2 and layer 3 switching capabilities. The device is built around a flexible FPGA device, offering long term feature enhancements, upgrades, and fixes, as well as a complete firmware development environment for custom applications.

Figure 1: The Cisco Nexus 3550-T Triton

The hardware platform specifications of the Nexus 3550-T are as follows:

- 1RU 48 port SFP28 (Small Form-factor Pluggable 28) configuration (backwards compatible with SFP+ and SFP).
- Dual redundant, hot-swap PSUs and dual hot-swap fans.
- Build using a Xilinx Virtex Ultrascale Plus VU35P Field Programmable Gate Array (FPGA) with a “-3” speed grade. The chip has 8GB of High Bandwidth Memory (HBM) on board.
- x86-based management processor with 100MB/s/1GB/s (RJ45) and 1GB (SFP+) based management ports.
- Hardware (electronics) supporting 25G speeds to the FPGA.

Ease of Management

The Cisco Nexus 3550-T Programmable Network Platform features a console port, a Micro USB port, and a 1G RJ45 port, which can be used as management interfaces. The Cisco Nexus 3550-T Platform uses a Command Line Interface (CLI) designed to address the needs of low-latency FPGA configurations.

The Cisco Nexus 3550-T Programmable Network Platform includes standard enterprise manageability and deployment capability features such as automatic configuration (via DHCP), SNMP, TACACS+ authentication, on-board Python programmability, BASH shell access, and time-series logging.

Please refer https://www.cisco.com/c/en/us/td/docs/dcn/nexus3550/3550-t/sw/101x/configuration/cisco-nexus-3550t-configuration-guide.html to learn more.

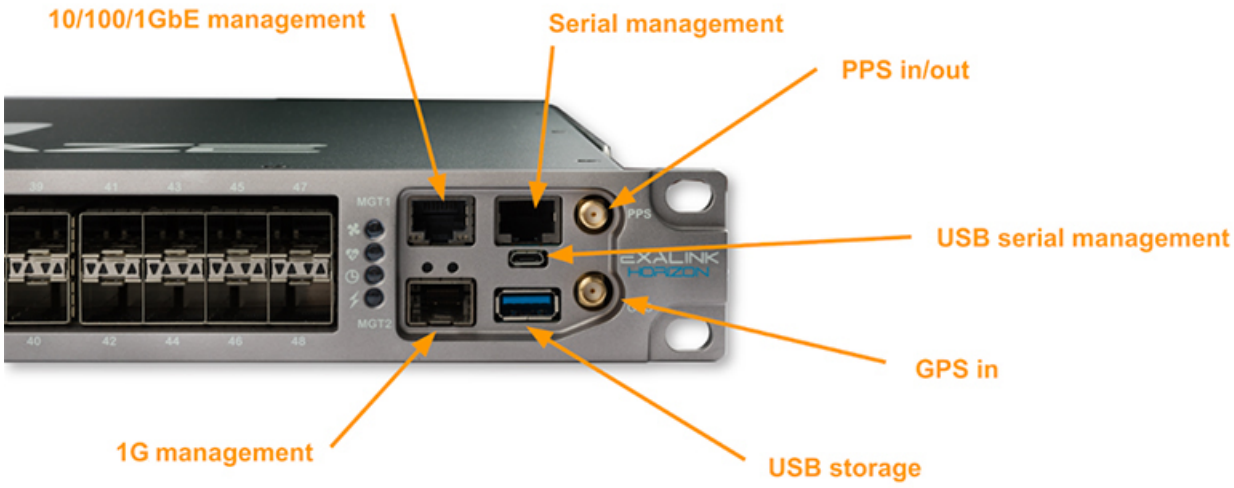
Hardware Architecture of the Cisco Nexus 3550-T Switches

The FPGA in the Cisco Nexus 3550-T is a Xilinx Virtex UltraScale+ HBM xcvu35p-fsvh2892-3-e.

The X86 processor in the Nexus 3550-T platform is an Intel Atom C3708 SoC, built into a third-party System on Module (SoM). The CPU features 8 cores, running at 1.7Ghz with 16MB of cache. There is 16GB of DDR4 Memory on the SoM, and the system boots from an M.2 NVMe SSD drive, with 128GB of non-volatile storage. There is a spare (unpopulated) M.2 drive bay available.

A block diagram of the Nexus 3550-T platform is given below.

Figure 2: Cisco Nexus 3550-T Hardware Architecture



Features

The Cisco Nexus 3550-T Programmable Network Platform has a fixed form factor that is built around a dynamically reconfigurable FPGA (Field Programmable Gate Array) and provides 48 ports along with an x86 (Intel® Atom® processor with 8 cores up to 1.7 GHz)–management CPU. See the following table for details on the speed that is supported on the ports:

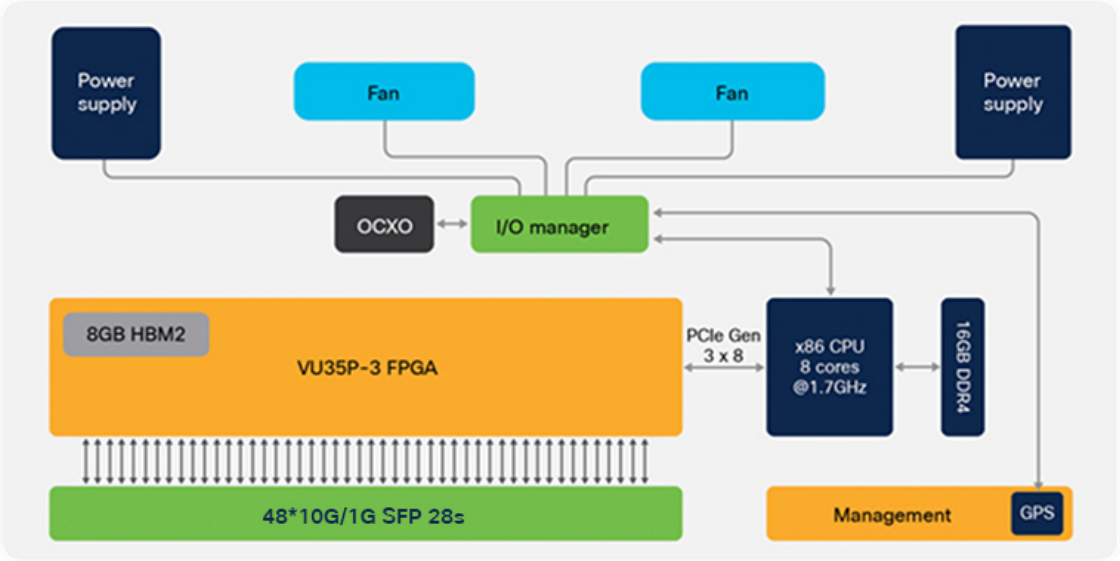
Table 1: Port speed table

Release	Port speed
10.2(3v)	All 48 ports support 1G/10G.

Release	Port speed
10.2(3t)	All 48 ports support 10G.

All 48 ports are directly connected to Xilinx Virtex UltraScale Plus VU35P FPGA with a “-3” speed grade. The FPGA has 8GB of High Bandwidth Memory (HBM) on board. The Cisco Nexus 3550-T hardware architecture diagram is shown in Figure 2 below.

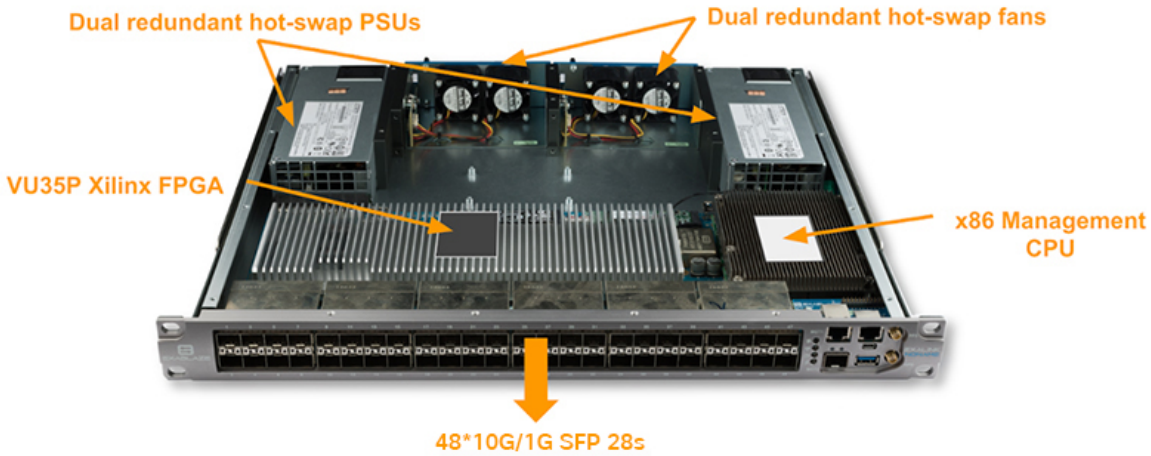
Figure 3: Cisco Nexus 3550-T Programmable Network Platform Data Sheet



Cisco Nexus 3550-T Programmable Network Platform hardware architecture

The Cisco Nexus 3550-T platform has a Xilinx Virtex Ultrascale Plus FPGA (XCVU35P-3e), 48 SFP ports (See Table 1: Port speed table) and an Intel Atom CPU. A firmware development kit is available from Cisco, enabling users with FPGA development capability to implement custom FPGA functionality in the XCVU35P-3e FPGA of the Cisco Nexus 3550-T.

Figure 4: The Cisco Nexus 3550-T Programmable Switch Platform Architecture



The FPGA module can run host of multiple firmware personalities. Currently, the following firmware versions are available:

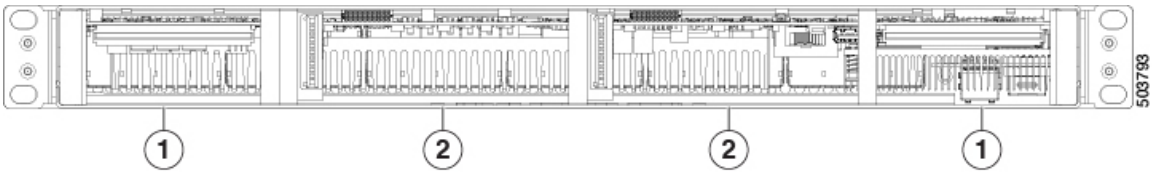
- **10G Layer 3 switch firmware:** With this firmware, the device operates as a 48-port low latency Layer 3 switch.

Initial 10G Layer 3 Switch Features

- Standard management interfaces: SNMP / TACACS+ / Syslog / JSON-RPC API
- Layer 2 switching features: MAC learning, VLAN tagging/trunking, LLDP, IGMP & STP
- Layer 3 switching features: IP routing, BGP, OSPF, and PIM
- Layer 4 switching features: Static NAT/PAT

The following figure shows the fan-side chassis features that you use when installing the chassis or replacing its modules.

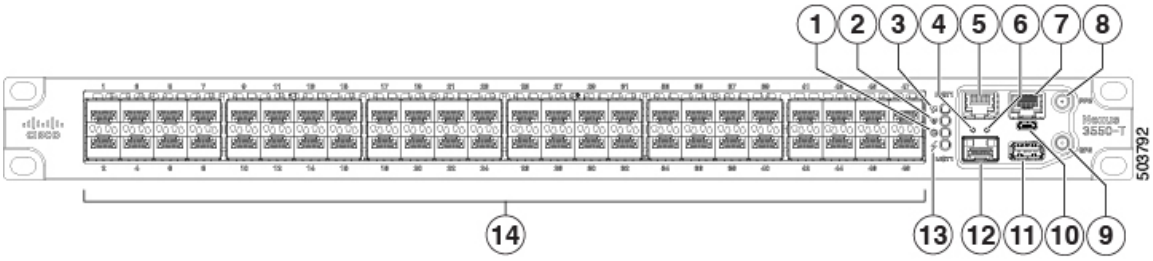
Figure 5: Fan-Side View of the Cisco Nexus 3550-T Chassis



1	Fan modules (1 and 1)	2	AC power supply (2 and 2)

The following figure shows the port-side chassis features that you use when installing the chassis or replacing its modules.

Figure 6: Port-Side View of the Cisco Nexus 3550-T Chassis



1	Management, Console, and USB ports	2	48 fixed small form-factor pluggable (SFP+) ports

Please refer https://www.cisco.com/c/en/us/td/docs/dcn/nexus3550/3550-t/sw/101x/configuration/cisco-nexus-3550t-configuration-guide.html to learn more.