



# ASUS NUC 13 Rugged Board / Kit

## Technical Product Specification

Regulatory Models: NUC13BRK (Slim Kit)

NUC13BRF (Tall Kit)

NUC13BRB (Board)

*Mar 2024  
Revision 5.0*

ASUS NUC Boards NUC13BR may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata, if any, are documented in ASUS NUC Board NUC13BR Specification Update.

# Revision History

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**Table 1. Revision History**

<b>Revision</b>	<b>Revision History</b>	<b>Date</b>
1.0	Draft release of the ASUS NUC 13 Rugged Board/Kit Technical Product Specification	May 2023
2.0	Rebranding Logo and Labels update	Oct. 2023
3.0	Summary feature update	Nov. 2023
4.0	Board Layout Update & rebranding updates	Dec. 2023
5.0	Product Identification Info and CPU operating temp update	Mar. 2024

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# Preface

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This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for ASUS NUC Rugged NUC13BR Board/Kits. Some features are only available on certain SKUs.

## Intended Audience

The TPS is intended to provide detailed, technical information about ASUS NUC Rugged NUC13BR Board and Kit, and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

## What This Document Contains

**Table 2. Document Contents Description**

Chapter	Description
1	An overview of the features and specifications of the ASUS NUC 13 Rugged NUC13BR
2	The figures, layouts, and physical description of the ASUS NUC 13 Rugged NUC13BR Board
3	Detailed descriptions of the features and specifications
4	Technical references and considerations
5	An overview of BIOS features and specifications

## Typographical Conventions

This section contains information about the conventions used in this specification. Not all these symbols and abbreviations appear in all specifications of this type.

## Notes, Cautions, and Warnings



### **NOTE**

*Notes call attention to important information.*



### **CAUTION**

*Cautions are included to help you avoid damaging hardware or losing data.*

## Other Common Notation

**Table 3. Common Notations**

#	Used after a signal name to identify an active-low signal (such as USBP0#)
GB	Gigabyte (1,073,741,824 bytes)
GB/s	Gigabytes per second
Gb/s	Gigabits per second
KB	Kilobyte (1024 bytes)
Kb	Kilobit (1024 bits)
kb/s	1000 bits per second
MB	Megabyte (1,048,576 bytes)
MB/s	Megabytes per second
Mb	Megabit (1,048,576 bits)
Mb/s	Megabits per second
TDP	Thermal Design Power
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.
x.x A	Amperes.
*	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

# Board Identification Information

## Basic ASUS NUC Board NUC13BRK Identification Information

Table 4. Board/BIOS Identification

AA Revision	BIOS Revision	Notes
	BRADL0036.00XX	1
	BRADL0036.00XX	1

Notes:

1. The AA number is found on a small label on the component side of the board.

# Production Identification Information

**Table 5. ASUS NUC Products NUC13BR Identification Information**

<b>Product Name</b>	<b>ASUS NUC Board</b>	<b>Processor</b>
NUC13BRK	NUC13BRKP2	Intel® Processor N50
NUC13BRF	NUC13BRFA2	Intel® Atom® x7211E
	NUC13BRBA2	
NUC13BRB	NUC13BRBA4	Intel® Atom® x7425E
	NUC13BRFA4	

# Specification Changes or Clarifications

The table below indicates the Specification Changes or Specification Clarifications that apply to the ASUS NUC Rugged NUC13BR Board and Kit.

## Specification Changes or Clarifications

**Table 6. Specification Changes**

Date	Type of Change	Description of Changes or Clarifications

## Errata

Current characterized errata, if any, are documented in a separate Specification Update. See for the latest documentation.

## Online Support

### To Find Information About...

ASUS NUC Board/Kit/Rugged PC  
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# 1 Product Description

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## 1.1 Overview

### 1.1.1 Summary of Standard Kit and Board SKUs

Product Codes and MM#s for the SKUs below can be found at <https://www.asus.com/support/>

**Table 7. Summary of Standard Kits and Board SKUs**

Processor	Chassis	AC Cord (C5)	
Intel® Processor N50 (Config A) Technology	Slim	US, EU, CN, TW, JP, or No Cord	
	Tall	US, EU, or No Cord	
Intel Atom® Processor X7211E (Config B)	Slim	US, EU, or No Cord	
	Tall	US, EU, CN, TW, JP, or No Cord	
	Board	N/A	
Intel Atom® Processor X7425E (Config C)	Slim	US, EU, or No Cord	
	Tall	US, EU, CN, TW, JP, or No Cord	
	Board	N/A	

<sup>1</sup>“TW” refers to Taiwan | <sup>2</sup>“CN” refers to China | <sup>3</sup>“JP” refers to Japan

## 1.1.2 Feature Summary Kits

**Table 8 Summarizes the major features of the ASUS NUC Rugged NUC13BR Boards and Kits**

**Table 8. Feature Summary**

<b>Board Dimensions</b>	146mm x 101.7mm
<b>Max Chassis Dimensions</b>	Slim chassis: 174mm x 108mm x 25.9mm (+3.4mm rubber feet) Tall chassis: 174mm x 108mm x 35.8mm (+3.4mm rubber feet)
<b>Processor</b>	ASUS NUC 13 Rugged Boards and Kits have a soldered-down Alder-Lake-N processor from the list below. <ul style="list-style-type: none"> <li>• Intel® Processor N50 (Config A)</li> <li>• Intel Atom® Processor X7211E (Config B)</li> <li>• Intel Atom® Processor X7425E (Config C)</li> </ul> More information about Intel® processors can be found at <a href="https://ark.intel.com">https://ark.intel.com</a>
<b>Memory</b>	1 x Single Channel DDR5-4800 SODIMM <ul style="list-style-type: none"> <li>• Support for In-band ECC capability</li> <li>• With 8Gb or 16 Gb capacity</li> </ul> More information about tested memory can be found at <a href="https://www.asus.com/support/">https://www.asus.com/support/</a>
<b>Graphics</b>	Integrated graphics support for processors with Intel® Graphics Technology: <ul style="list-style-type: none"> <li>• Supports up to dual 4K@60Hz display or dual 1080@60Hz (2 x HDMI 2.1 TMDS)</li> <li>• HDR (High Dynamic Range) support</li> <li>• Dual display pipes – supporting blending, color adjustments, scaling, and dithering.</li> <li>• Support for HDCP 2.3</li> <li>• Codecs supported are detailed in Section 3.1 3.1</li> <li>• Support Headless, 2<sup>nd</sup> Virtual Display and Persistent Display Mode Operation</li> </ul>
<b>Audio</b>	The processor supports the following audio formats over HDMI*: HBR Dolby TrueHD and DTS-HD Master Audio More information about software and drivers can be found at <a href="https://www.asus.com/support/Download-Center/">https://www.asus.com/support/Download-Center/</a>
<b>Storage</b>	One M.2 PCIe x2 connector supporting M.2 22x80 (key type M) for NVMe only. One 64GB eMMC
<b>Communication</b>	Intel® Wi-Fi 6E <sup>1</sup> AX210 (Gig+) M.2 2230 add-in card via M.2 2230 (key type E) connector <ul style="list-style-type: none"> <li>• 802.11ax R2 2x2, both with 160Mhz channel support + Bluetooth v5.3</li> <li>• Maximum transfer speed up to 2.4 Gbps</li> <li>• Supports PCIe and USB</li> </ul> More information about Intel® wireless products can be found at <a href="https://ark.intel.com">https://ark.intel.com</a> To obtain drivers visit <a href="https://www.asus.com/support/Download-Center/">https://www.asus.com/support/Download-Center/</a>  Dual 2.5 Gigabit (10/100/1000/2500 Mbps) Ethernet ports <ul style="list-style-type: none"> <li>• Intel® Ethernet Controller I226-V (SKU Dependent)</li> <li>• Intel® Ethernet Controller I226-LM (SKU Dependent)</li> <li>• Single-port integrated multi-gigabit (up to 2.5G) – standard IEEE 802.3 Ethernet interface for 2500BASE-T, 1000BASE-T, 100BASE-TX, 10BASE-TE connections (IEEE 802.3, 802.3u, 802.3bz, and 802.3ab)</li> <li>• Full wake up support (S4 WOL not supported)</li> <li>• Supports for packets up to 9.5 KB (Jumbo Frames)</li> </ul> More information about Intel® Ethernet controllers can be found at <a href="https://ark.intel.com">https://ark.intel.com</a>

<b>USB Ports and Headers</b>	<p>2 x USB 3.2 Gen2 port (rear panel)                  2 x USB 2.0 port (rear panel)                  2 x USB 2.0 Headers (internal)</p> <p>More information about the location of the USB ports and headers can be found in Section 3.6.3 later in this document.                  More information about the pinout of the USB ports and headers can be found in Section 3.4 later in this document</p>
<b>Power</b>	<p>Power Adapter</p> <ul style="list-style-type: none"> <li>• 65W adapter ADP 20V, 3.25A 3P DT VI</li> <li>• 90W adapter ADP 20V, 4.5A 3P DT VI</li> <li>• 90W adapter ADP 20V, 4.5A 3P DT VI</li> </ul> <p>Internal Power Header</p> <ul style="list-style-type: none"> <li>• 4-pos/dual row (2x2) right-angled header</li> </ul> <p>Power Input</p> <ul style="list-style-type: none"> <li>• 12V<sub>DC</sub> to 20V<sub>DC</sub> +/- 5% with DC voltage protection</li> </ul>
<b>Operating Temperatures</b>	<ul style="list-style-type: none"> <li>• Intel® Atom® x7211E 0 - 50 °C External Ambient Temp</li> <li>• Intel® Atom® x7425E 0 - 40 °C External Ambient Temp</li> <li>• Intel® Processor N50 0 - 40 °C External Ambient Temp</li> </ul>
<b>BIOS</b>	<p>ASUS BIOS resident in the Serial Peripheral Interface (SPI) Flash device</p> <ul style="list-style-type: none"> <li>• Support for Advanced Configuration and Power Interface (ACPI), Plug and Play</li> </ul>
<b>Supported Operating System</b>	<ul style="list-style-type: none"> <li>• Windows 10 IOT-Enterprise LTSC 64-bit</li> <li>• Ubuntu 22.04 LTS</li> <li>• RedHat Enterprise Linux 9</li> <li>• Windows 11 Pro 64-bit</li> </ul>
<b>Hardware Monitor Subsystem</b>	<p>Hardware monitoring subsystem including:                  Voltage sense to detect out of range power supply voltages.                  Thermal sense to detect out of range thermal values</p>
<b>Design for Rugged</b>	<ul style="list-style-type: none"> <li>• Rated IP50</li> <li>• Industrial Design</li> <li>• Fanless</li> </ul>

<sup>1</sup> May not be available in all countries.

**Table 9. Additional Features**

<b>MIPI Camera</b>	<p>ASUS NUC 13 Rugged NUC13BR supports 2x MIPI CSI Camera headers, which supports Vision Components or Paper Image off-the-shelf camera.</p>
<b>HDMI CEC API</b>	<p>Built-in support for HDMI CEC is available on both HDMI ports, which may be enabled in the BIOS for display power control, as well as via an API supporting other HDMI CEC functions.</p> <p>More information about the HDMI CEC API specification is available on <a href="https://www.intel.com/content/www/us/en/support/articles/000056864/intel-nuc.html">https://www.intel.com/content/www/us/en/support/articles/000056864/intel-nuc.html</a></p>
<b>Sustained Operation</b>	<p>Qualified for 24x7 sustained operation</p>
<b>Auto RTC Reset</b>	<p>A Real-Time Clock (RTC) reset is triggered after three consecutive unsuccessful boot attempts.</p>
<b>Delayed AC Start</b>	<p>Short delay after AC power is applied before unit is ready to power on to protect the system against voltage fluctuations in environments where multiple devices are being powered on simultaneously</p>
<b>Reflectivity</b>	<p>All surfaces meet 20GE (20 Gloss Level/Gloss Units) of shininess by measurement of Glanz</p>
<b>Kensington Security Slot</b>	<p>Available on the right side of the chassis when viewed from the front</p>
<b>Cable Locking Arm</b>	<p>ASUS NUC Rugged PCs and Kits NUC13BR ship with a cable locking arm on the back panel of the chassis. The cable locking arm reduces stress on the power adapter cable in certain positions and prevents unintended losses of power</p>
<b>LED Status Indicators</b>	<p>ASUS NUC 13 Rugged Kits feature three System Status LEDs to represent overall boot health (useful for headless deployments) as well as firmware/software robustness capabilities. There are three Network Status LEDs representing overall network connectivity.</p>

## 2 Product Layout

### 2.1 Board Layout

#### 2.1.1 Board Layout (BACK/FRONT PLANES)

Figure 1 and 2 shows the location of the major components on the bottom of ASUS NUC Board NUC13BRK/ NUC13BRF/NUC13BRB

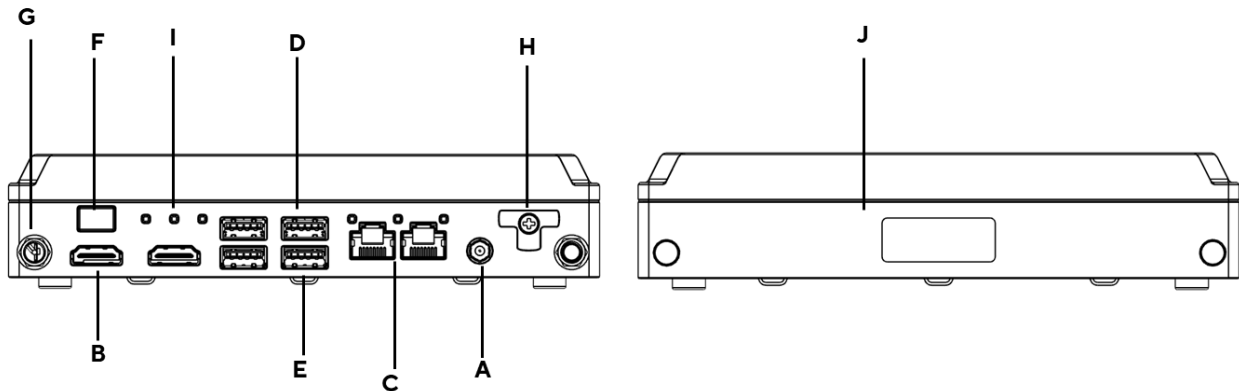
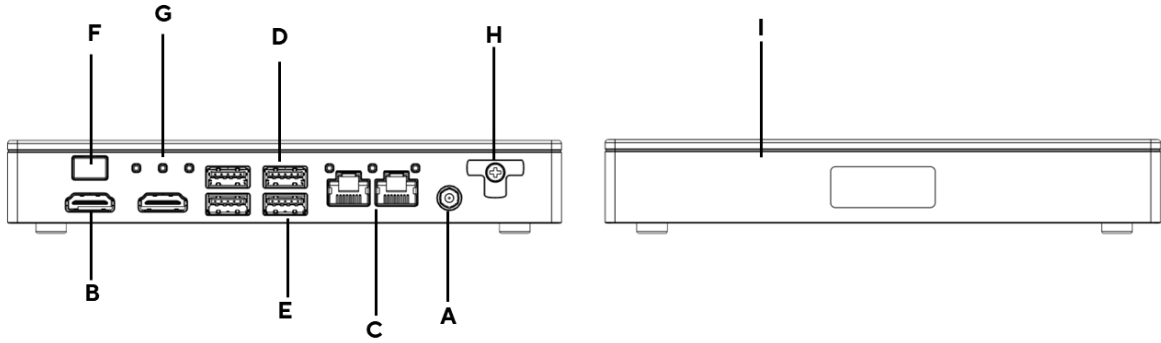


Figure 1. Tall Chassis Layout

Table 10. Components Shown in Figure 1. Tall Chassis Layout

Item from Figure 1	Description
A	12-20 V DC Input Jack
B	HDMI 2.1 TMDS Port 1 with Built-In CEC Support
C	LAN Connectors
D	Back Panel 2 USB 3.2 Gen 2
E	Back Panel 2 USB 2.0
F	Power Button
G	Antenna Connection
H	Cable Locking Arm
I	LEDs
J	Front Chassis image



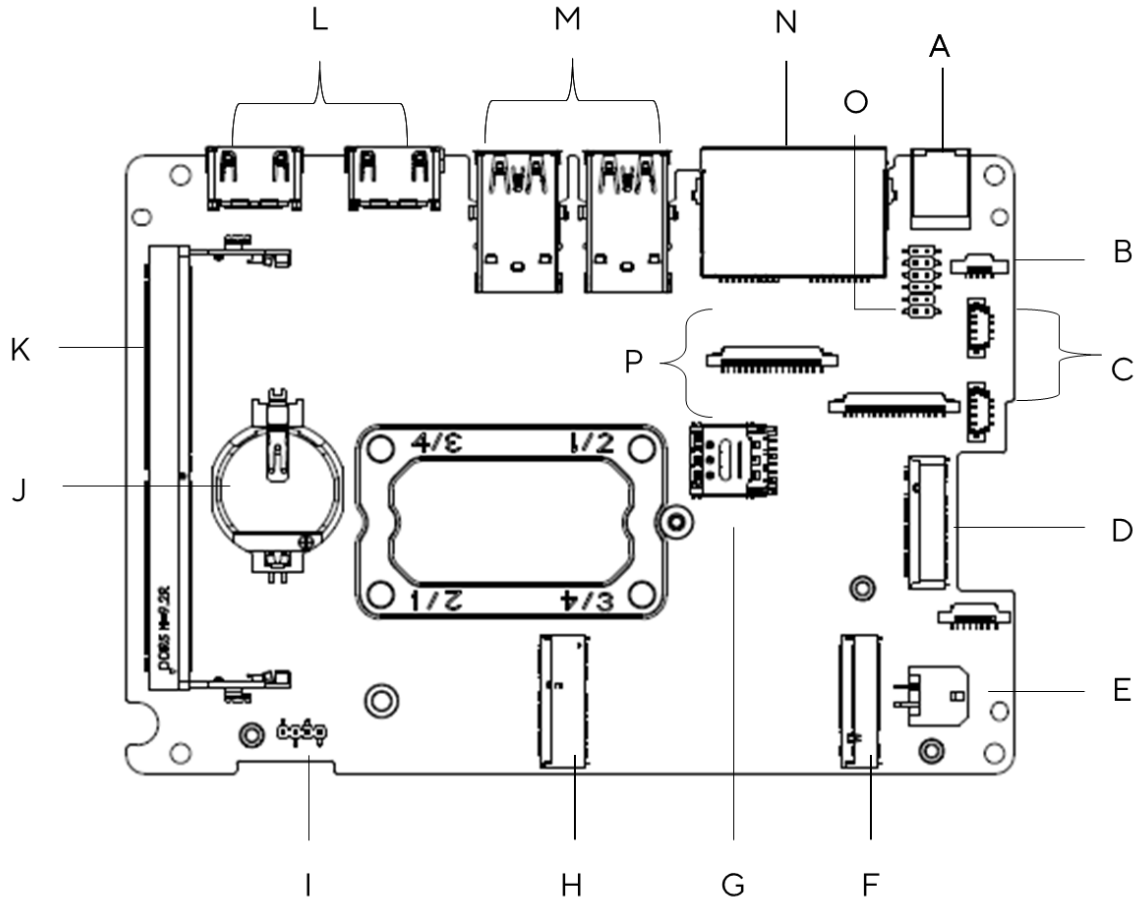
**Figure 2. Slim Chassis Layout**

**Table 11. Components Shown in Figure 2. Slim Chassis Layout**

Item from Figure 2	Description
A	12-20 V DC Input Jack
B	HDMI 2.1 TMDS Port 1 with Built-In CEC Support
C	LAN Connector
D	Back Panel 2 USB 3.2 Gen 2
E	Back Panel 2 USB 2.0
F	Power Button
G	LEDs
H	Cable Locking Arm
I	Front Chassis image

## 2.1.2 Board Layout (Top)

**Error! Reference source not found.**3 shows the location of the major components on the bottom-side of ASUS NUC Board NUC13BRK/ NUC13BRF/NUC13BRB



**Figure 3. Major Board Components (Top)**

**Table 12. Components Shown in Figure 3.**

Item from	Description
A	Power Connector (12V <sub>DC</sub> to 20V <sub>DC</sub> +/- 5% with DC voltage protection)
B	MIPI Header 3
C	USB Internal Header
D	M.2 Key B 3042

E	Internal Power Header
F	M.2 Key-M 2280
G	SIM Card Socket
H	M.2 Key E 2230
I	TGPIO Header
J	CMOS Battery Holder
K	DDR5 SODIMM Socket
L	HDMI Connectors
M	USB Type-A Connectors
N	RJ-45 LAN Ports
O	Front Panel Header
P	MIPI CSI

### 2.1.3 Block Diagram

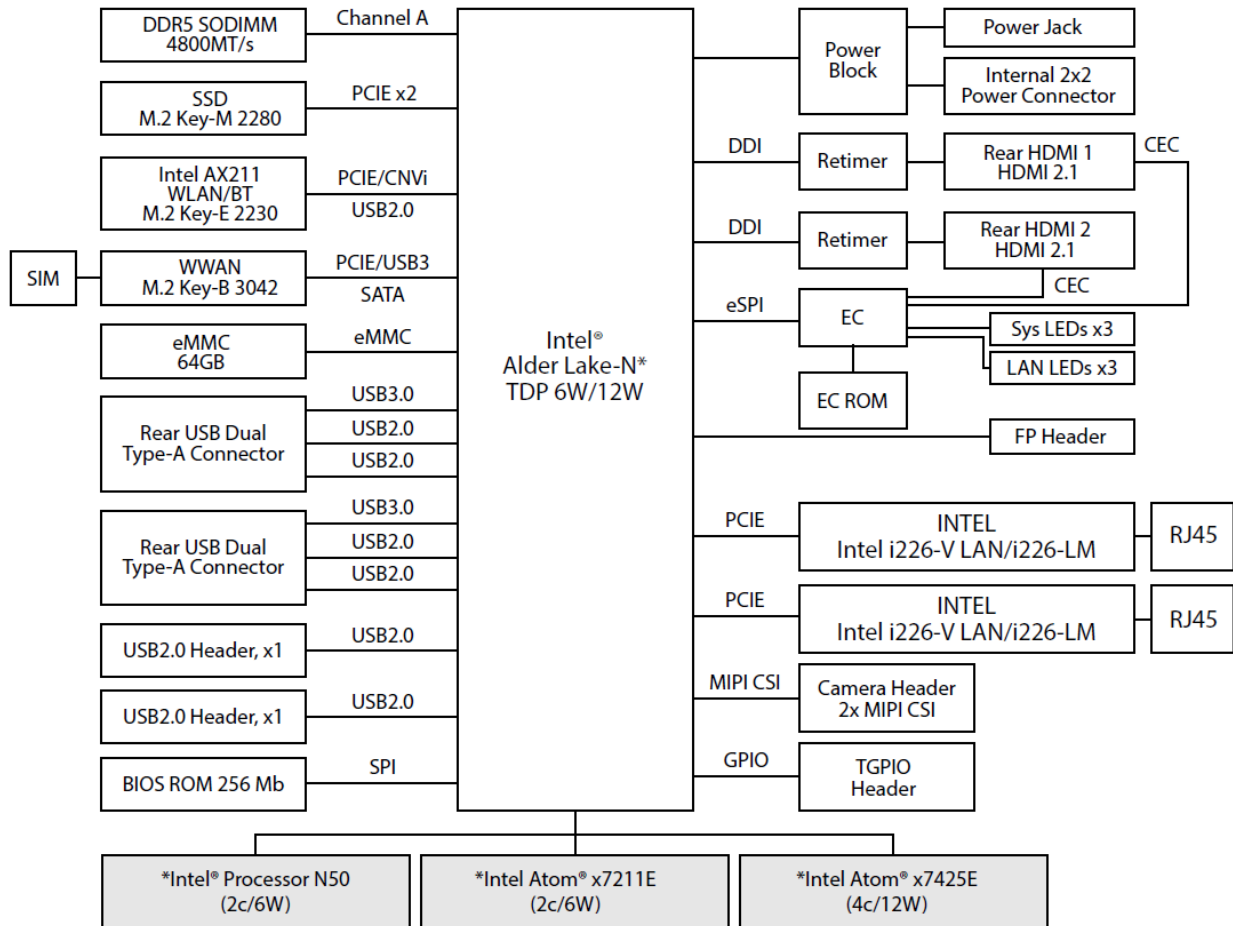


Figure 4. Block Diagram

## 2.1.4 Chassis Expandability Options

The chassis side panel of the ASUS NUC Rugged NUC13BR Boards and Kits Canyon supports an opening for 3rd party / customer expandability option. This expandability bay usage is not limited to, Camera connections, etc. The chassis provides a plastic face plate for covering the side panel opening when no expansion is installed. The Face plate matches the chassis color and texture. Some 3<sup>rd</sup> party expandability dongles are available from <https://gorite.com> and a specification is available for the design of 3<sup>rd</sup> party add in cards. This is the shipping configuration:

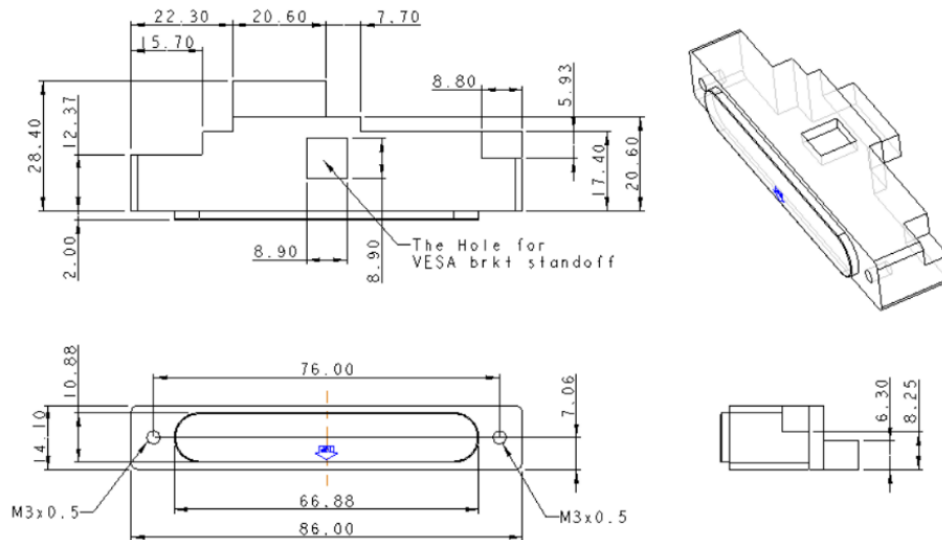


Figure 5. Tall Chassis Side Panel Expansion Slot

## 3 Feature Descriptions

### 3.1 Graphics Subsystem

ASUS NUC Boards NUC13BRK / NUC13BRF / NUC13BRB support Integrated graphics support for processors with Intel® Processor N50 and Intel Atom® Processors (X7211E and X7425E).

Integrated graphics support for processors with Intel® Graphics Technology:

- Supports up to dual 4K@60Hz display or dual 1080@60Hz (2 x HDMI 2.1 TMDS)
- HDR (High Dynamic Range) support
- Dual display pipes – supporting blending, color adjustments, scaling, and dithering.
- Support for HDCP 2.3
- Codecs supported are detailed in Section 3.1 or <https://www.asus.com/support/Download-Center/>

- Support Headless, 2nd Virtual Display and Persistent Display Mode Operation
- Accelerate Video Processing for Visual Experiences, Video Walls, and Graphics- Intensive Apps

Integrated graphics create new opportunities for visually rich experiences and graphics-enhanced controls while reducing dependency on discrete graphics hardware. 13th Gen Intel® Core™ processors featuring Intel® UHD Graphics 770 driven by Intel® Xe architecture<sup>4</sup>—with up to 16 graphics execution units (EUs) for N50 Processor, X7211E Processor and 24 graphics execution units for X7425E Processor, — deliver fast graphics performance. Three display pipes of 4K60 HDR video, up to three multiformat codec (MFX) engines—up to 2x video decode and 1x video encode—and Genlock and Pipelock support video walls, digital signage, and processing for multiple video streams.

Several of the featured technologies in the 13th Gen platform are designed to support industrial and telecommunications applications that demand more reliability, bounded-latency workloads, and robust wireless connectivity. Select SKUs of 13th Gen Intel® processors support:

- Intel® Time Coordinated Computing (TCC)
- Time- Sensitive Networking (TSN) capability with integrated, real-time-capable 2x 2.5GbE connections. This is supported on i226-LM SKUs only.

Select SKUs also bring support for embedded use conditions and discrete Intel® Wi-Fi 6E connectivity. These featured technologies are especially useful where wired connections or physical access to a device is otherwise inconvenient or costly.

## 3.1.1 Display Emulation

Display emulation is supported using the HDMI ports so that the system may be remotely accessed in a headless configuration or be capable of tolerating display connectivity interruptions without the operating system redetecting and rearranging the overall display layout. The display emulation feature may be enabled in BIOS Setup with the following checkboxes:

- “Virtual display emulation”: provides a 1280x1024 virtual display when no displays are connected to the system and provides an additional 1280x1024 virtual display if one display is attached to the system. If two displays are attached to the HDMI ports, these displays are enabled, and no virtual displays are provided.
- “Persistent display emulation”: emulates that both displays are always connected to the system no matter their actual connection status. The EDID information from each display remains programmed through S3, S4, S5 and G3 power states until the feature is disabled.
  - When “Persistent display emulation” is enabled another drop-down menu (“Inconsistent Display Device”) becomes visible that allows the user to select the behavior of the system when the display device EDID is inconsistent with the EDID stored by the system.
    - “Block boot” (default selection): the BIOS displays a warning message with options and waits indefinitely for a user selection.
    - “Countdown”: the BIOS displays a warning message with options and waits 10 seconds before booting.



### NOTE

*When using “Persistent display emulation” it would be expected behavior for the system not to properly drive displays different than those connected when the feature was enabled, as the EDID parameters of the initially connected displays are still being driven by the system. In order to retrain the system for different displays, the persistent display emulation feature must be disabled in the BIOS, the system rebooted, and then the persistent display emulation feature must be reenabled.*

## 3.2 NVMe/SATA Interfaces

The PCH provides three Internal M.2 interface slots with a theoretical maximum transfer rate and provides the following interfaces:

- M.2 #1 22x80 supports up to 3.5 Gb/s with one PCIe M.2 slot for SSD and AI accelerator use. The M.2 SSD slot is required to support NVMe drives.
- M.2 #2 22x30 support up to 2.4 Gb/s with one M.2 slot for wireless card expandability. L10 SKU is equipped with a wireless card pre-installed. However, board SKUs have an empty slot.
- M.2 #3 30x42 up to 6 Gb/s is designed to have one 30x42 B-keyed M.2 slot which is used for WWAN, SATA, NVMe (NVMe x2 running as NVMe x1 only) and AI accelerator expansion module.



### NOTE

*Bravo Canyon is not equipped with a 2.5" SATA Drive Bay.*

## 3.3 Real-Time Clock Subsystem

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to  $\pm 13$  minutes/year at 25 °C with 3.3 VSB applied via the power supply 5 V STBY rail.



### NOTE

*If the battery and AC power fail, date and time values are reset and the user is notified during the POST.*

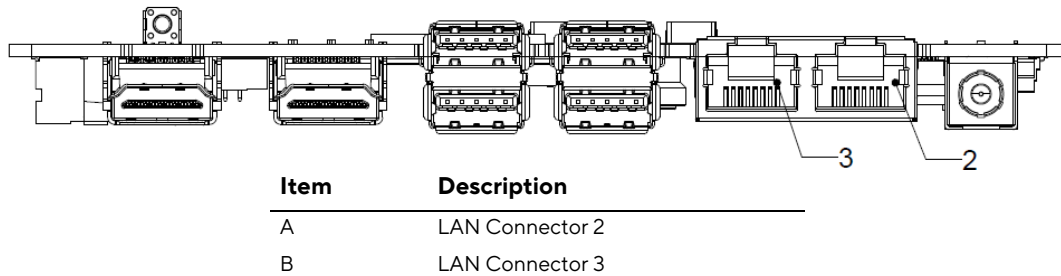
*When the voltage drops below a certain level, the BIOS Setup program settings stored in CMOS RAM (for example, the date and time) might not be accurate. Replace the battery with an equivalent one. **Error! Reference source not found.** on page **Error! Bookmark not defined.** shows the location of the battery.*

*System can power on from G3/AC power loss state without the Real-Time Clock battery.*

## 3.4 LAN Subsystem

### 3.4.1 RJ-45 LAN Connector with Integrated LEDs

Two LEDs are built into the RJ-45 LAN connector (shown in **Figure 6. LAN Connectors Location 6**).



**Figure 6. LAN Connectors Location**

Table 13 describes the LED states when the board is powered up and the LAN subsystem is operating.

**Table 13. LAN Connector LED States**

LED	LED Color	LED State	Condition
Link	Green	Off	LAN link is not established
		Solid	LAN link is established
		Blinking	LAN activity is occurring
Data Rate	Green/Yellow	Off	10/100 Mb/s data rate is selected
		Yellow	1000 Mb/s data rate is selected
		Green	2500 Mb/s data rate is selected

## 3.5 MIPI CSI Interfaces

### 3.5.1 The pin out of the multiple MIPI headers

0.5mm FPC Camera Header			
Function	NUC Pin	Description	Note
MIPI CSI-2 Signals	1	GND	
	2	CSI_DAT0_N	
	3	CSI_DAT0_P	
	4	GND	
	5	CSI_DAT1_N	
	6	CSI_DAT1_P	
	7	GND	
	8	CSI_CLK_N	
	9	CSI_CLK_P	
	10	GND	
	11	CSI_DAT2_N	
	12	CSI_DAT2_P	
	13	GND	
	14	CSI_DAT3_N	
	15	CSI_DAT3_P	
	16	GND	
	17	CSI_CLK_N	
	18	CSI_CLK_P	
	19	GND	
Driver Defined GPIO Functions	20	PWM1 / GPIO1	1.8v PCH PWM1/GPIO1
	21	PWM2 / GPIO2	1.8v PCH PWM2/GPIO2
	22	GPIO3	1.8v PCH GPIO3
	23	GPIO4	1.8v PCH GPIO4
	24	CLK1 / GPIO5	1.8v PCH CLK1/GPIO5
	25	CLK2 / GPIO6	1.8v PCH CLK2/GPIO6
	26	GND	
I2C	28	I2C_SDA	1.8v LVTT/LVCMOS
	29	I2C_SCL	1.8v LVTT/LVCMOS
Cam PWR	27	Vcc3V3	0.5A
	30	Vcc3V3	0.5A

Figure 7. PIN Out of MIPI Headers

### 3.5.2 Enable the MIPI CSI Interfaces in BIOS Menu

To enable the MIPI CSI Interfaces, users need to modify BIOS configurations in BIOS setup menu following below instructions.

1. Enable IPU Device and 1181 Dash Camera in BIOS menu -> Advanced -> MIPI Camera.



2. Configure camera **HID** and **GPIO** settings in BIOS menu -> Advanced -> MIPI Camera -> Slot1 or Slot2. Default camera settings are for **INTC10C0** and **IMX415** cameras.



3. If 3<sup>rd</sup> party camera modules are used, users need to customize camera **HID** and **GPIO** settings in BIOS menu -> Advanced -> MIPI Camera -> Slot1 or Slot2.



## 3.6 Hardware Management Subsystem

### 3.6.1 Fanless Thermal Solution

The chassis is required to be fanless, thermally and environmentally robust in lower air-quality environments (i.e., dust, 40°C ambience, etc.). Bravo will not be used outdoors.

Fan-less thermal solution meets these requirements:

- The chassis and thermal solution need to be designed so all system configurations do not exceed 70C skin temp at 35C ambient.
- We can exceed 70C skin temperature at higher ambience. The ODM must perform testing at 40C and 50C for respective configurations to inform ASUS of the max skin temp observed under the PRD defined workloads.
- Warning labels and or notifications is provided to customers if skin temps exceed 80C under ambient conditions > 35C.

### 3.6.2 System States and Power States

Table 14 describes the ACPI states supported by the processor.

#### 3.6.2.1 Wake-up Devices and Events

**Lists devices or specific events that can wake the computer from specific states.**

Bravo Canyon must support the wake-up events listed below. Note that S4 implies OS support only.

**Table 14. LAN Wake Events**

Wake-Up Event	State from Sleep
Power button	S3, S4, S5
RTC alarm	S3, S4, S5
LAN	S3, S5
USB	S3, S4, S5
PCIe	S3, S4
Bluetooth	S3, S4
WiFi	S3, S4, S5
WWAN	S3, S4, S5



#### **NOTE**

*The use of these wake-up events from an ACPI state requires an operating system that provides full ACPI support. In addition, software, drivers, and peripherals must fully support ACPI wake events.*

### 3.6.3 Signal Tables for the Connectors and Headers

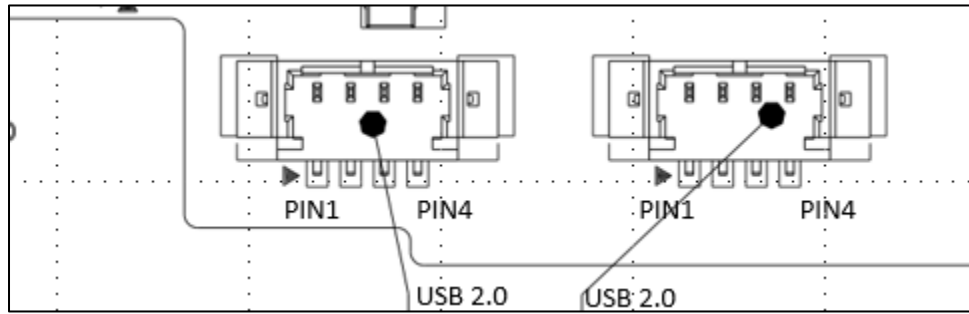


Figure 8. USB Header PIN Layout

Table 15. Internal USB 2.0 Headers (1.25 mm pitch)

Pin	Signal Name
1	5 V <sup>1</sup>
2	D -
3	D +
4	GND

<sup>1</sup> The two USB 2.0 headers on the board can deliver 1A per port.

Connector is Molex part number 53398-0471, 1.25mm Pitch PicoBlade\* Header, Surface Mount, Vertical, Lead-Free, 4 Circuits.

Table 16. M.2 2280 Module (Mechanical Key M) Connector

#	Requirement	Details																								
1	Slot form Factor	22x80																								
2	Number of Slots	3																								
3	SSD Support	PCIe Gen4 NVMe																								
4	Slot Type	Socket 3, key M; Must meet Gold plating requirements in 2.6.28																								
5	Slot Post and screw	Post w/Philips-head screw installed @ 80mm Torque for post in 80mm solder nut: 2.5±0.5 in-lbs Torque for screw in post: Must be slightly less than torque setting above. Unscrewing screw from post must not cause post to loosen Screw is to have ferromagnetic properties for ease of assembly.																								
6	Power Delivery Requirement	3.3VDC @ 3.5A nominal, 7.0A peak																								
7	Slot Signals	<table border="1"> <thead> <tr> <th>Pin</th> <th>Signal Name</th> <th>Pin</th> <th>Signal</th> </tr> </thead> <tbody> <tr> <td>74</td> <td>3.3V</td> <td>75</td> <td>GND</td> </tr> <tr> <td>72</td> <td>3.3V</td> <td>73</td> <td>GND</td> </tr> <tr> <td>70</td> <td>3.3V</td> <td>71</td> <td>GND</td> </tr> <tr> <td>68</td> <td>SUSCLK(32kHz) (O)(0/3.3V)</td> <td>69</td> <td>PEDET (NC-PCIe/GND-SATA)</td> </tr> <tr> <td>66</td> <td>Connector Key</td> <td>67</td> <td>N/C</td> </tr> </tbody> </table>	Pin	Signal Name	Pin	Signal	74	3.3V	75	GND	72	3.3V	73	GND	70	3.3V	71	GND	68	SUSCLK(32kHz) (O)(0/3.3V)	69	PEDET (NC-PCIe/GND-SATA)	66	Connector Key	67	N/C
Pin	Signal Name	Pin	Signal																							
74	3.3V	75	GND																							
72	3.3V	73	GND																							
70	3.3V	71	GND																							
68	SUSCLK(32kHz) (O)(0/3.3V)	69	PEDET (NC-PCIe/GND-SATA)																							
66	Connector Key	67	N/C																							

		64	Connector Key	65	Connector Key
		62	Connector Key	63	Connector Key
		60	Connector Key	61	Connector Key
		58	N/C	59	Connector Key
		56	N/C	57	GND
		54	PEWAKE# (I/O)(0/3.3V) or N/C	55	REFCLKP
		52	CLKREQ# (I/O)(0/3.3V) or N/C	53	REFCLKN
		50	PERST# (O)(0/3.3V) or N/C	51	GND
		48	N/C	49	PETp0
		46	N/C	47	PETn0
		44	N/C	45	GND
		42	N/C	43	PERp0
		40	N/C	41	PERn0
		38	DEVSLP(O)	39	GND
		36	N/C	37	PETp1
		34	N/C	35	PETn1
		32	N/C	33	GND
		30	N/C	31	PERp1
		28	N/C	29	PERn1
		26	N/C	27	GND
		24	N/C	25	N/C
		22	N/C	23	N/C
		20	N/C	21	GND
		18	3.3V	19	N/C
		16	3.3V	17	N/C
		14	3.3V	15	GND
		12	3.3V	13	N/C
		10	DAS/DSS# (I/O)/LED1# (I)(0/3.3V)	11	N/C
		8	PLN	9	GND
		6	N/C	7	N/C
		4	3.3V	5	N/C
		2	3.3V	3	GND
				1	GND
<b>8</b>	iRST PCIe Remapping support	Required			

**Table 17. M.2 2230 Module (Mechanical Key E) Connector**

#	Requirement	Details																																																
1	Slot form Factor	M.2 22x30 - <a href="http://www.pcisig.com/members/downloads/PCIe_M.2_Electromechanical_Spec_Rev1.0_Final_11012013_RS_Clean.pdf">http://www.pcisig.com/members/downloads/PCIe_M.2_Electromechanical_Spec_Rev1.0_Final_11012013_RS_Clean.pdf</a>																																																
2	Number of Slots	1																																																
3	Slot Type	Key "E"; must meet Gold plating requirements in section 2.6.28.																																																
4	Slot Nut, Post	1x solder nut installed @ 30mm position, pre-installed with 1x post w/wireless card installed in the 22x30 slot.																																																
5	Power Delivery Requirement	3.3V <sub>DC</sub> @ 2.75A																																																
6	Slot Signals	<table border="1"> <thead> <tr> <th>Pin</th> <th>Signal Name</th> <th>Pin</th> <th>Signal Name</th> </tr> </thead> <tbody> <tr> <td>74</td> <td>3.3V</td> <td>75</td> <td>GND</td> </tr> <tr> <td>72</td> <td>3.3V</td> <td>73</td> <td>WT_CLKP</td> </tr> <tr> <td>70</td> <td>UIM_POWER_SRC/GPIO1/PEWAKE1#</td> <td>71</td> <td>WT_CLKN</td> </tr> <tr> <td>68</td> <td>CLKREQ1#</td> <td>69</td> <td>GND</td> </tr> <tr> <td>66</td> <td>PERST1#</td> <td>67</td> <td>WTD0P</td> </tr> <tr> <td>64</td> <td>REFCLK0</td> <td>65</td> <td>WTD0N</td> </tr> <tr> <td>62</td> <td>ALERT#/A4WP_IRQ# (I)(0/3.3)</td> <td>63</td> <td>GND</td> </tr> <tr> <td>60</td> <td>I2C_CLK/A4WP_I2C_CLK (O)(0/3.3)</td> <td>61</td> <td>WT_D1P</td> </tr> <tr> <td>58</td> <td>I2C_DATA/A4WP_I2C_DATA (I/O)(0/3.3)</td> <td>59</td> <td>WT_D1N</td> </tr> <tr> <td>56</td> <td>W_DISABLE1# (O)(0/3.3V)</td> <td>57</td> <td>GND</td> </tr> <tr> <td>54</td> <td>W_DISABLE2# (O)(0/3.3V)</td> <td>55</td> <td>PEWAKE0# (I/O)(0/3.3V)</td> </tr> </tbody> </table>	Pin	Signal Name	Pin	Signal Name	74	3.3V	75	GND	72	3.3V	73	WT_CLKP	70	UIM_POWER_SRC/GPIO1/PEWAKE1#	71	WT_CLKN	68	CLKREQ1#	69	GND	66	PERST1#	67	WTD0P	64	REFCLK0	65	WTD0N	62	ALERT#/A4WP_IRQ# (I)(0/3.3)	63	GND	60	I2C_CLK/A4WP_I2C_CLK (O)(0/3.3)	61	WT_D1P	58	I2C_DATA/A4WP_I2C_DATA (I/O)(0/3.3)	59	WT_D1N	56	W_DISABLE1# (O)(0/3.3V)	57	GND	54	W_DISABLE2# (O)(0/3.3V)	55	PEWAKE0# (I/O)(0/3.3V)
Pin	Signal Name	Pin	Signal Name																																															
74	3.3V	75	GND																																															
72	3.3V	73	WT_CLKP																																															
70	UIM_POWER_SRC/GPIO1/PEWAKE1#	71	WT_CLKN																																															
68	CLKREQ1#	69	GND																																															
66	PERST1#	67	WTD0P																																															
64	REFCLK0	65	WTD0N																																															
62	ALERT#/A4WP_IRQ# (I)(0/3.3)	63	GND																																															
60	I2C_CLK/A4WP_I2C_CLK (O)(0/3.3)	61	WT_D1P																																															
58	I2C_DATA/A4WP_I2C_DATA (I/O)(0/3.3)	59	WT_D1N																																															
56	W_DISABLE1# (O)(0/3.3V)	57	GND																																															
54	W_DISABLE2# (O)(0/3.3V)	55	PEWAKE0# (I/O)(0/3.3V)																																															

52	PERSTO# (O)(0/3.3V)	53	CLKREQ0# (I/O)(0/3.3V)
50	SUSCLK(32kHz) (O)(0/3.3V)	51	GND
48	COEX1 (I/O)(0/1.8V)	49	REFCLKNO
46	COEX2 (I/O)(0/1.8V)	47	REFCLKPO
44	COEX3 (I/O)(0/1.8V)	45	GND
42	CLink_CLK (I/O); NC for SR project	43	PERn0
40	CLink_DATA (I/O); NC for SR project	41	PERp0
38	C-Link RESET* (I) (0/3.3V); NC for SR project	39	GND
36	UART RTS/BRI_DT (I) (0/1.8V)	37	PETn0
34	UART CTS (O) (0/1.8V)	35	PETp0
32	UART TXD/RGI_DT (I) (0/1.8V)	33	GND
30	Connector Key	31	Connector Key
28	Connector Key	29	Connector Key
26	Connector Key	27	Connector Key
24	Connector Key	25	Connector Key
22	UART RXD/BRI_RSP (O) (0/1.8V)	23	WGR_CLKP
20	UART WAKE# (O) (0/3.3V)	21	WGR_CLKN
18	GND/LNA_EN	19	GND
16	LED2#	17	WGR_DOP
14	PCM_OUT/I2SSD_OUT/CLKREQ0	15	WGR_DON
12	PCM_IN/I2SSD_IN	13	GND
10	PCM_SYNC/I2SWS/RF_RESET_B	11	WGR_D1P
8	PCM_CLK/I2SSCK	9	WGR_D1N
6	LED1#	7	GND
4	3.3V	5	USB_D-
2	3.3V	3	USB_D+
		1	GND

**Table 18. M.2 30x42 Module (Mechanical Key B) Connector**

Bravo Canyon has one M.2 30x42 slot for wireless card expandability that's pre-installed. See section 3.6.3.1 for additional detailed information.

		CONFIG_2	75
74	3.3V	GND	73
72	3.3V	GND	71
70	3.3V	CONFIG_1	69
68	SUSCLK(32kHz) (O)(0/3.3V)	RESET# (O)(0/1.8V)	67
66	SIM DETECT (O)	ANTCTL3 (I)(0/1.8V)	65
64	COEX1 (I/O)(0/1.8V)	ANTCTL2 (I)(0/1.8V)	63
62	COEX2 (I/O)(0/1.8V)	ANTCTL1 (I)(0/1.8V)	61
60	COEX3 (I/O)(0/1.8V)	ANTCTL0 (I)(0/1.8V)	59
58	N/C	GND	57
56	N/C	REFCLKP	55
54	PEWAKE# (I/O)(0/3.3V)	REFCLKN	53
52	CLKREQ# (I/O)(0/3.3V)	GND	51
50	PERST# (O)(0/3.3V)	PETp0/SATA-A+	49
48	GPIO_4 (I/O)(0/1.8V*)	PETn0/SATA-A-	47
46	GPIO_3 (I/O)(0/1.8V*)	GND	45
44	GPIO_2 (I/O)(0/1.8V*)	PERp0/SATA-B-	43
42	GPIO_1 (I/O)(0/1.8V*)		

40	GPIO_0 (I/O)(0/1.8V*)	PERn0/SATA-B+	41
38	DEVSLP (O)	GND	39
36	UIM-PWR (I)	PETp1/USB3.0-Tx+/SSIC-TxP	37
34	UIM-DATA (I/O)	PETn1/USB3.0-Tx-/SSIC-TxN	35
32	UIM-CLK (I)	GND	33
30	UIM-RESET (I)	PERp1/USB3.0-Rx+/SSIC-RxP	31
28	GPIO_8 (I/O) (0/1.8V)	PERn1/USB3.0-Rx-/SSIC-RxN	29
26	GPIO_10 (I/O) (0/1.8V)	GND	27
24	GPIO_7 (I/O) (0/1.8V)	DPR (O) (0/1.8V)	25
22	GPIO_6 (I/O)(0/1.8V)	GPIO_11 (I/O) (0/1.8V)	23
20	GPIO_5 (I/O)(0/1.8V)	CONFIG_0	21
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
10	GPIO_9/DAS/DSS# (I/O)/LED1#(I)(0/3.3V)	GND	11
8	W_DISABLE1# (O)(0/3.3V)	USB_D-	9
6	FULL_CARD_POWER_OFF# (O)(0/1.8V or 3.3V)	USB_D+	7
4	3.3V	GND	5
2	3.3V	GND	3
		CONFIG_3	1

**3.6.3.1 M.2 30x42 Pin-Out (Mechanical Key B) detail info**

- Socket 2 pinout is intended to support WWAN+GNSS, SSD, and other types of Add-In solutions with the defined and configurable Host I/Fs.
- WWAN can make use of USB2.0, USB3.0, PCIe (up to two Lanes), or SSIC host I/Fs. The actual implemented I/F is identified through the Configuration pins state (1 of 16 states) on the Module side. LED1# and W\_DISABLE1# are intended for use with the WWAN solution. There are additional WWAN and GNSS related pins including W\_DISABLE2#, DPR, and WAKE\_ON\_WWAN#
- The UIM and SIM Detect pin are used in conjunction with a SIM device in support of the WWAN solution.
- The COEX and ANTCTL pins are placeholders for future expansion and definition of these functions.
- The GPIO0..11 pins are configurable with four different variants. These variants can be in support of the GNSS interface, second UIM/SIM, Audio interfaces, HSIC and IPC sidebands. The exact definition is determined by which configuration was identified by decoding the four Configuration pins.

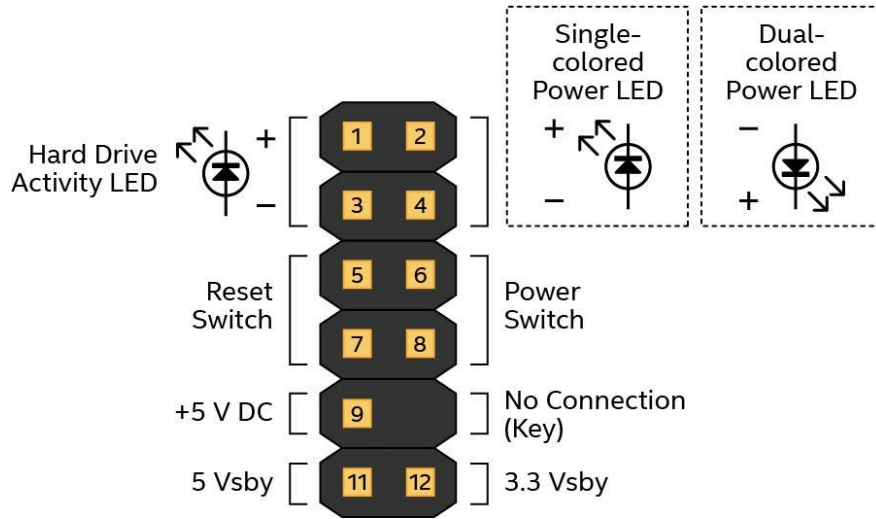
- The FULL\_CARD\_POWER\_OFF# and the RESET# pins are unique and intended to be used when the WWAN solution is plugged into platforms that provide a direct connection to VBATT (and not a regulated 3.3 V) such as Tablet platforms. They are not used in NB and Very thin notebooks type platforms that provide a regulated 3.3 V power rail. But the FULL\_CARD\_POWER\_OFF# signals should be tied to the 3.3V power rail on the NB/very thin platform.
- The SSD can make use of the PCIe two Lanes or overlaid SATA host I/F. The actual implemented I/F is identified through the CONFIG\_1 pin state (1 or 0) in conjunction with the other three Configuration pin states that are all 0. DAS/DSS# (overlaid on the LED1#) and DEVSLP are intended for use with the SATA SSD solution.
- The SUSCLK pin provides a Slow Clock signal of 32 kHz to enable Low Power States.
- Pins labeled N/C should Not Be Connected.

### 3.6.3.2 Back Panel Header (2.0 mm Pitch)

This section describes the functions of the front panel header. Error! Reference source not found. **19** lists the signal names of the front panel header. Error! Reference source not found. **9** is a connection diagram for the front panel header.

**Table 19. Back Panel Header (2.0 mm pitch)**

Pin	Signal Name	Description	Pin	Signal Name	Description
1	HDD_POWER_LED	Pull-up 750Ω to +5V	2	POWER_LED_MAIN	[Out] Front panel LED (main color) Pull-up 300Ω to +5V
3	HDD_LED#	[Out] HDD activity LED	4	POWER_LED_ALT	[Out] Front panel LED (alt color)
5	GROUND	Ground	6	POWER_SWITCH#	[In] Power switch
7	RESET_SWITCH#	[In] Reset switch	8	GROUND	Ground
9	+5V_DC (1A) (Vcc)	VCC5 (1A current rating)	10	Key	No pin
11	5Vsby (2A)	5VSB (2A current rating)	12	3.3Vsby (1A)	3VSB (1A current rating)



**Figure 9. Connection Diagram for Front Panel Header (2.0 mm Pitch)**

**3.6.3.2.1 Hard Drive Activity LED Header**

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. Proper LED function requires a SATA hard drive or optical drive connected to an onboard SATA connector.

**3.6.3.2.2 Reset Switch Header**

Pins 5 and 7 can be connected to a momentary single pole, single throw (SPST) type switch that is normally open. When the switch is closed, the board resets and runs the POST.

**3.6.3.2.3 Power/Sleep LED Header**

Pins 2 and 4 can be connected to a one- or two-color LED. Error! Reference source not found. **20** and **Table 21** show the possible LED states.

**Table 20. States for a One-Color Power LED**

LED State	Description
Off	Power off
Blinking	Standby
Steady	Normal operation

**Table 21. States for a Dual-Color Power LED**

LED State	Description
Off	Power off
Blinking (white)	Standby
Steady (white)	Normal operation



## NOTE

The LED behavior shown in is default – other patterns may be set via BIOS setup.

### 3.6.3.2.4 Power Switch Header

Pins 6 and 8 can be connected to a front panel momentary-contact power switch. The switch must pull the SW\_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off (the time requirement is due to internal debounce circuitry on the board). At least two seconds must pass before the power supply recognizes another on/off signal.

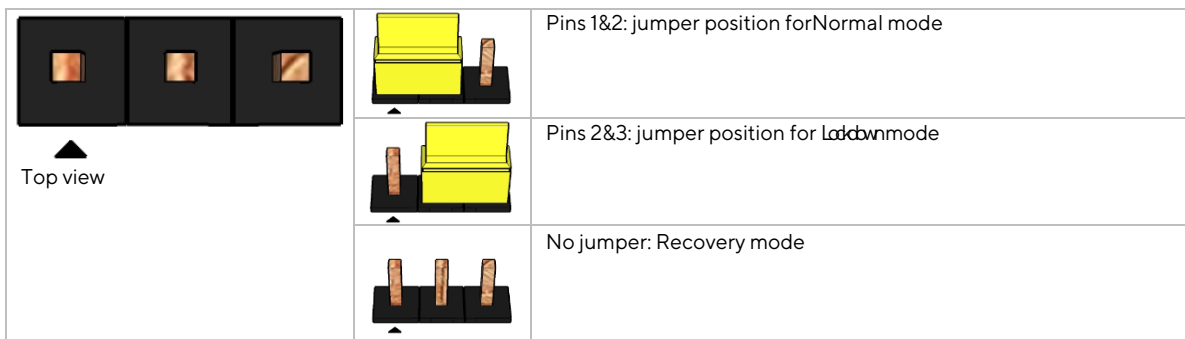
### 3.6.3.3 BIOS Security Jumper



## CAUTION

Do not move a jumper with the power on. Always turn off the power and unplug the power cord from the computer before changing the jumper setting. Otherwise, the board could be damaged.

Figure 10: Shows the location of the BIOS Security Jumper. The Pins1&2 and Pins 2&3 jumpers determine the BIOS Security program’s mode.



**Figure 10. BIOS Security Jumper Header**

Table 22 describes the jumper settings for the three modes: normal, lockdown, and configuration.

**Table 22. BIOS Security Jumper Settings**

Function/Mode	Jumper Setting	Configuration
Normal	1-2	The BIOS uses current configuration information and passwords for booting.

Lockdown	2-3	<p>The BIOS uses current configuration information and passwords for booting, except:</p> <ul style="list-style-type: none"> <li>• All POST Hotkeys are suppressed (prompts are not displayed and keys are not accepted. For example, F2 for Setup, F10 for the Boot Menu).</li> <li>• Power Button Menu is not available (see Section 3.6.3.2 Power Button Menu).</li> </ul> <p>BIOS updates are not available except for automatic Recovery due to flash corruption.</p>
Configuration	None	<p>BIOS Recovery Update process if a matching *.bio file is found. Recovery Update can be cancelled by pressing the Esc key.</p> <p>If the Recovery Update was cancelled or a matching *.bio file was not found, a Config Menu is displayed. The Config Menu consists of the following (followed by the Power Button Menu selections):</p> <ul style="list-style-type: none"> <li>[1] Suppress this menu until the BIOS Security Jumper is replaced.</li> <li>[2] Clear BIOS User and Supervisor Passwords.</li> <li>[3] Reset ASUS AMT to default factory settings.</li> <li>[F2] ASUS Visual BIOS.</li> <li>[F4] BIOS Recovery.</li> </ul> <p>See Section 4.3.2 Power Button Menu</p>



**NOTE** The ASUS NUC Rugged NUC13BR Boards and Kits do not support discrete TPM.

### 3.6.3.4 Power Supply Connectors



**NOTE** External power voltage, 12-20 (±5%) V DC, is dependent on the type of power supply used. System power requirements depend on actual system configurations chosen by the integrator, as well as end user expansion preferences. It is the system integrator’s responsibility to ensure an appropriate power budget for the system configuration is properly assessed based on the system-level components chosen.



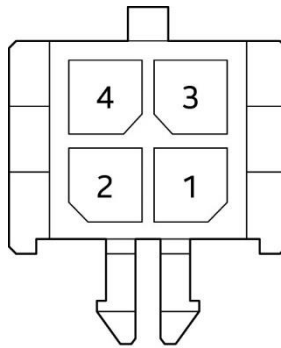
#### CAUTION

There is no isolation circuitry between the external DC jack and the internal 2 x 2 power connector. It is the system integrator’s responsibility to ensure no more than one power supply unit is or can be attached to the board at any time and to ensure the external DC jack is covered if the internal 2 x 2 power connector is to be used. Simultaneous connection of both external and internal power supply units could result in potential damage to the board, power supplies, or other hardware.

The board has the following power supply connectors:

- **External Power Supply** – the board can be powered through a 12-20 V DC connector on the back panel. The back-panel DC connector is compatible with a 5.5 mm/OD (outer diameter) and 2.5 mm/ID (inner diameter) plug, where the inner contact is +12-20 V DC, and the shell is GND. The maximum current rating is 10 A.
- **Internal Power Supply** – the board can alternatively be powered via the internal 12-20 V DC 2 x 2 power connector, where pins 1 and 2 are +12-20 V DC and pins 3 and 4 are GND. The maximum current rating is 10 A (5A per pins 1 and 2).

The connector used is Molex Micro-Fit (3mm pitch), right-angled, 4-pos/dual row (2x2).



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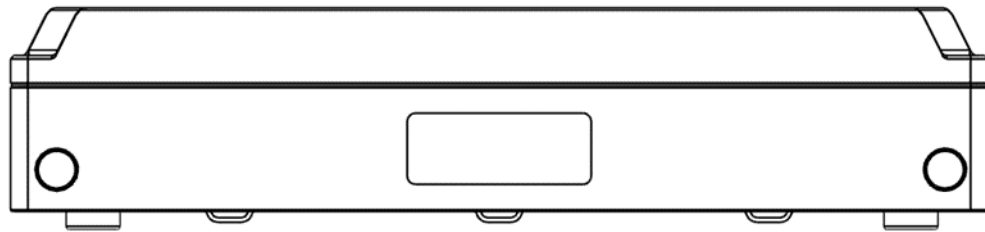
**Table 23. Internal Power Supply Connector Pins**

Pins	Signal Name
1,2	+12-20V
3,4	GND

**Figure 11. Connection Diagram for the Internal Power Supply Connector**

## 3.7 Mechanical Considerations

### 3.7.1 Chassis Images



**Figure 12. Tall Chassis Image Front**

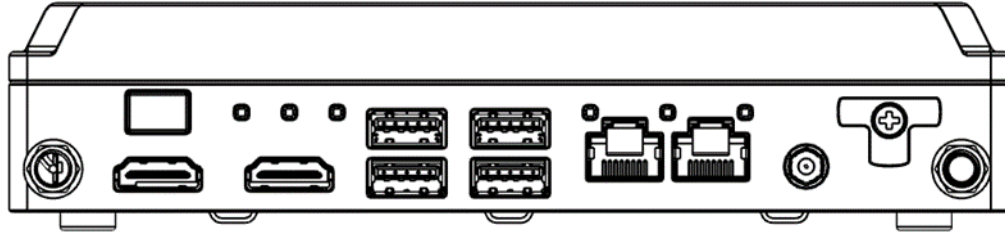


Figure 13. Tall Chassis Image Back



Figure 14. Short Chassis Image Front

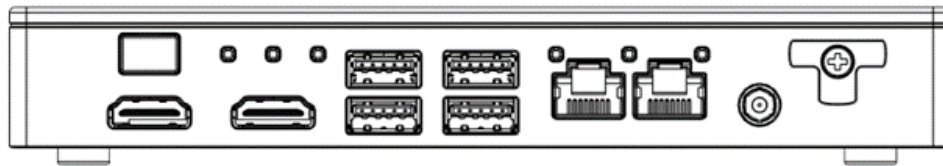


Figure 15. Short Chassis Image Back

### 3.8 Thermal Considerations



**CAUTION**

*Failure to ensure appropriate airflow may result in reduced performance of both the processor and/or voltage regulator or, in some instances, damage to the board.*

*All responsibility for determining the adequacy of any thermal or system design remains solely with the system integrator. ASUS makes no warranties or representations that merely following the instructions presented in this document results in a system with adequate thermal performance.*



**CAUTION**

*Ensure that the ambient temperature does not exceed the board's maximum operating temperature. Failure to do so could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 3.10.*



## **CAUTION**

*Ensure that proper airflow is maintained in the processor voltage regulator circuit. Failure to do so may result in a shorter than expected product lifetime.*

### **3.9 Reliability**

The demonstrated Mean Time Between Failures (MTBF) is done through 24/7 testing. Full ASUS NUC systems in chassis with memory, SSD or HDD, and a fan are run at 100% on time for 90 days continuously while running system wide stress inducing software in a 40 °C ambient air temperature chamber. The demonstrated MTBF for ASUS NUC Board NUC13AN / NUC13LC is >50,000 hours.

### 3.10 Environmental

Table 24 lists the environmental specifications for the board.



#### CAUTION

*If the external ambient temperature exceeds 50 °C, further thermal testing is required to ensure components do not exceed their maximum operating temperature.*

**Table 24. Environmental Specifications**

Parameter	Specification
<b>Temperature</b>	
Sustained Storage Limits (i.e., warehouse)	-20 °C to +40 °C
Short Duration Limits (i.e., shipping)	-40 °C to +60 °C

\* Processor performance may automatically decrease when the system operates in the top 5 °C of the ambient operating temperature ranges above. This is for local ambient temperature inside the ASUS NUC Rugged NUC13BR Board/Kits chassis.

Intel® Processor N50 (2c/6W)	0 °C to +40 °C Ambient Operating Temp for Kit and Board SKU
Intel Atom® x7211E (2c/6W)	0 °C to +50 °C Ambient Operating Temp for Kit and Board SKU
Intel Atom® x7425E (4c/12W)	0 °C to +40 °C Ambient Operating Temp for Kit and Board SKU

<b>Shock (Board)</b>			
Unpackaged		50 g trapezoidal waveform	
		Velocity change of 170 inches/s <sup>2</sup>	
Packaged		Free fall package drop machine set to the height determined by the weight of the package.	
	Product Weight (pounds)	Non-palletized Product drop height (inches)	Palletized drop heights (single product) (inches)
	<20	36	N/A
	21-40	30	N/A
	41-80	24	N/A
	81-100	18	12
	100-120	12	9

<b>Shock (System)</b>	
Unpackaged	
25g trapezoidal waveform	
Velocity = 250 inches/sec, 2 shock table drops in each of 6 directions	

<b>Vibration (Board)</b>	
Unpackaged	Random profile 5 Hz @ 0.01 g <sup>2</sup> /Hz to 20 Hz @ 0.02 g <sup>2</sup> /Hz (slope up) 20 Hz to 500 Hz @ 0.02 g <sup>2</sup> /Hz (flat)
	Input acceleration is 3.13g RMS
<b>Vibration (System)</b>	
Unpackaged	Random profile 5 Hz @ 0.001 g <sup>2</sup> /Hz to 20 Hz @ 0.01 g <sup>2</sup> /Hz (slope up) 20 Hz to 500 Hz @ 0.01 g <sup>2</sup> /Hz (flat)
	Input acceleration is 2.20g RMS
Packaged	Random Profile: 0.001 g <sup>2</sup> /Hz to 20 Hz @ 0.01 g <sup>2</sup> /Hz (slope up) 20 Hz to 500 Hz @ 0.01 g <sup>2</sup> /Hz (flat)
	Input acceleration is 2.20g RMS

Note: The operating temperature of the board may be determined by measuring the air temperature from the junction of the heatsink fins and fan, next to the attachment screw, in a closed chassis, while the system is in operation.

Note: Before attempting to operate this board, the overall temperature of the board must be above the minimum operating temperature specified. It is recommended that the board temperature be at least room temperature before attempting to power on the board. The operating and non-operating environment must avoid condensing humidity.

## 4 Overview of BIOS Features

### 4.1 Introduction

The board uses an ASUS AMI BIOS core that is stored in the Serial Peripheral Interface Flash Memory (SPI Flash) and can be updated through multiple methods (see Section 4.2). The SPI Flash contains the BIOS Setup program, POST, the PCI auto-configuration utility, LAN EEPROM information, and Plug and Play support. The SPI Flash includes a 32 MB flash memory device.

The BIOS Setup program can be used to view and change the identification information and the BIOS settings for the system. The BIOS Setup program is accessed by pressing <F2> after the POST memory test beings and before the operating system boots.

### 4.2 BIOS Updates

The BIOS can be updated using one of the following methods:

1. Express BIOS (Windows-based) Update
2. F7 Update
3. Power Button Menu Update
4. UEFI Shell Update

More information and instructions on how to use each of these methods can be found at [BIOS Update and Recovery Instructions](#). All BIOS update files for ASUS NUCs are available on [Download Center](#).

## 4.2.1 BIOS Recovery

It is unlikely that anything will interrupt a BIOS update; however, if an interruption occurs the BIOS could be unstable. **Error! Reference source not found.** lists the drives and media types that can be used for BIOS recovery. The BIOS recovery media does not need to be made bootable. More information about BIOS recovery methods and instructions can be found at [BIOS Update and Recovery Instructions](#).

**Table 25. Acceptable Drives/Media Type for BIOS Recovery**

Media Type <sup>(Note)</sup>	Can be used for BIOS recovery?
Hard disk drive (connected to SATA or USB)	Yes
USB flash drive	Yes
NVME SSD (M.2 interface)	Yes



**NOTE** Supported file systems for BIOS recovery: NTFS (sparse, compressed, or encrypted files are not supported), FAT32, EXT

## 4.3 Boot Options

In the BIOS Setup program, the user can choose to boot from a hard drive, removeable driver, or the network. The default setting is for the hard drive to be the first boot device, the removeable drive second, and the network third.



**NOTE** The network can be selected as a boot device. This selection allows booting from the onboard LAN or a network add-in card with a remote boot ROM installed. Pressing the <F12> key during POST automatically forces booting from the LAN. To use this key during POST, the User Access Level in the BIOS Setup program's Security menu must be set to Full.

### 4.3.1 Boot Device Selection During Post

Pressing the <F10> key during POST causes a boot device menu to be displayed. The menu displays the list of available boot devices.

### 4.3.2 Power Button Menu

As an alternative to Configuration Mode or normal POST hotkeys, the user can use the power button to access a menu with BIOS and boot options. The Power Button Menu is accessible via the following sequence:

1. System is in S4/S5 (not G3).
2. The user pushes the power button and holds it down for 3 seconds.
3. The Power Button LED will be white color for the first 3 seconds. After 3 seconds, switch the Power Button LED to yellow color to signal the user to release the power button.
4. User releases the power button before the 4-second shutdown override.

If this boot path is taken, the BIOS uses default settings, ignoring settings in VPD where possible. At the point where Setup Entry/Boot would be in the normal boot path, the BIOS displays the following prompt and wait for a keystroke:

If an unrecognized key is hit, then the BIOS does nothing and waits for another keystroke. If one of the listed hotkeys is hit, the BIOS will follow the indicated boot path. Password requirements must still be honored.

**Table 26. Power Button Menu Options**

Keystroke	Option	Description
[ESC]	Normal Boot	
[F2]	BIOS Setup Menu	
[F3]	Disable Fast Boot	Note: Is only be displayed if at least one Fast Boot optimization is enabled. If Disable Fast Boot is selected, the BIOS disables all Fast Boot optimizations and reset the system.
[F4]	BIOS Recovery	The BIOS searches for a matching .CAP file from the \EFI\ASUS folder in the supported media with the supported file system. If a matching recovery capsule is found, the BIOS displays the following: <b>BIOS Recovers to &lt;BIOSID&gt; in 20 seconds.</b> <b>[ESC] Cancel Recovery</b>

		Recovery proceeds if not cancelled via the ESC key within 20 seconds. The BIOS displays the recovery progress. If a BIOS .CAP file was not detected (or the BIOS Recovery was cancelled) then the BIOS resets the system and continues normally to POST.
[F5]	Restore BIOS Settings	The BIOS restores the current setup settings and the current defaults to the build time defaults in the case of a boot issue caused by setup variable changes.

## 4.4 Hard Disk Drive Password Security Feature

The Hard Disk Drive Password Security feature blocks read and write access to the hard disk drive until the correct password is given. Hard disk drive passwords are set in BIOS Setup and are prompted for BIOS POST. For convenient support for resuming from S3, the system BIOS automatically unlocks drives on resume from S3. Valid password characters are A-Z, a-z, and 0-9. Passwords may be up to 32 characters in length.

The User hard disk drive password, when set, is required on each power cycle until the Master Key or User hard disk drive password is submitted.

The Master Key hard disk drive password, when set, will not lock the drive. The Master Key hard disk drive password exists as an unlock override if the User hard disk drive password is forgotten. Only the User hard disk drive password, when set, causes a hard disk to be locked on a system power cycle. show the effects of setting the hard disk drive passwords.

**Table 27. Master Key and User Hard Disk Drive Password Functions**

Password Set	Password During Boot
Neither	None
Master only	None
User only	User only
Master and User Set	User

During every POST, if a User hard disk drive password is set, POST execution pauses with the following prompt to force the User to enter the Master Key or the User hard disk drive password:

**“Enter Hard Disk Drive Password:”**

Upon successful entry of the Master Key or User hard disk drive password, the system proceeds with normal POST.

If the hard disk drive password is not correctly entered, the system goes back to the above prompt. The User has three attempts to correctly enter the hard disk drive password. After the third unsuccessful attempt, the system halts with the following message:

**“Hard Disk Drive Password Entry Error”**

A manual power cycle is required to resume system operation.



**NOTE** As implemented on the ASUS NUC13AN / NUC13LC board, the hard disk drive password security feature is only supported on the SATA Port 0 (M.2) or the SATA port 1 (onboard SATA connector).

## 4.5 BIOS Security Features

BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A Supervisor and User password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The Supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is Supervisor Mode.
- The User password gives restricted access to view and change Setup options in the BIOS Setup program. This is User Mode.
- If only the Supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the Supervisor and User passwords are set, users can enter either the Supervisor or User password to access Setup. Users have access to Setup regardless of which password is used.
- Setting the User password restricts who can boot the computer. The password prompt is displayed before the computer boots. If only the Supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.
- For enhanced security, use different passwords for the Supervisor and User passwords.
- Valid password characters are A-Z, a-z, 0-9, and special characters. Passwords may be up to 20 characters in length.
- To clear a set password, enter a blank password after entering the existing password.

Table 28 shows the effects of setting the Supervisor password and User password. This table is for reference only and is not displayed on the screen.

**Table 28. Supervisor and User Password Functions**

<b>Password Set</b>	<b>Supervisor Mode</b>	<b>User Mode</b>	<b>Setup Options</b>	<b>Password to Enter Setup</b>	<b>Password During Boot</b>
Neither	Any user can change all options	Any user can change all options	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and User set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or User	Supervisor or User

## 4.6 BIOS Error Messages

Table 29 lists the error messages and provides a brief description of each.

**Table 29. BIOS Error Messages**

<b>Error Message</b>	<b>Explanation</b>
CMOS Battery Failure	The battery may be losing power. Replace the battery soon.
CMOS Checksum Error	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed, then the memory may be bad.
CMOS Timer Not Set	The battery may be losing power. Replace the battery soon.
Processor Thermal Trip	Processor overheated.
Auto RTC Reset	The system triggers RTC clear to recover the system back to normal condition from consecutive boot failure.

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