

## 280-0339-00-AO

Cyan® 280-0339-00 Compatible TAA OTU4/100GBase-LR4 CFP Transceiver (SMF, 1310nm, 10km, LC, DOM)

### Features

- CFP MSA 1.4 Compliance
- Commercial Temperature 0 to 70 Celsius
- Duplex LC Connector
- Hot Pluggable
- Excellent ESD Protection
- Single-mode Fiber
- RoHS Compliant and Lead Free
- Metal with Lower EMI



### Applications

- OTU4/100GBase Ethernet
- Access and Enterprise

### Product Description

This Cyan® 280-0339-00 compatible CFP transceiver provides 100GBase/OTU4-LR4 throughput up to 10km over single-mode fiber (SMF) using a wavelength of 1310nm via an LC connector. It is guaranteed to be 100% compatible with the equivalent Cyan® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."



## Absolute Maximum Ratings

| Parameter                        | Symbol | Min. | Max. | Unit |
|----------------------------------|--------|------|------|------|
| Storage Temperature              | TS     | -40  | +85  | °C   |
| Power Supply Voltage             | VCC    | -0.5 | 3.6  | V    |
| Operating Case Temperature Range | Tc     | -10  | +75  | °C   |
| Relative Humidity                | Rh     | 5    | 85   | %    |

## Electrical Characteristics

| Parameter                      | Symbol   | Min. | Typ. | Max. | Unit  |         |
|--------------------------------|----------|------|------|------|-------|---------|
| Power Supply Voltage           | VCC      | 3.2  | 3.3  | 3.4  | V     |         |
| Power Supply Current           | Icc      |      | 4000 |      | mA    |         |
| <b>Transmitter</b>             |          |      |      |      |       |         |
| Differential data input swing  | Vin      |      |      | 1050 | mVp-p |         |
| Input differential impedance   | Zin      | 80   | 100  | 120  | Ω     |         |
| <b>Receiver</b>                |          |      |      |      |       |         |
| Differential data output swing | Vout, pp | 360  |      | 770  | mVp-p |         |
| Output differential impedance  | Zo       | 80   | 100  | 120  | Ω     |         |
| Output Rise/Fall Time          | tr/tf    | 24   |      |      | ps    | 20%~80% |

## 1.2V MDIO Interface Specifications

| Parameter          | Symbol       | Min. | Typ. | Max   | Unit | Notes |
|--------------------|--------------|------|------|-------|------|-------|
| Input Voltage      | VIH          | 0.84 |      | 1.5   | V    |       |
|                    | VIL          | -0.3 |      | 0.36  | V    |       |
| Input Leak current | IIN          | -100 |      | 100   | uA   |       |
| Output Voltage     | VOH          | 1.0  |      | 1.5   | V    |       |
|                    | VOL          | -0.3 |      | 0.2   | V    |       |
| Input Capacitance  | CI           |      |      | 10    | pF   |       |
| Input MDC Clock    | fMDC         | 0.1  |      | 4     | MHz  |       |
| MDC Clock Period   | TMDC         | 250  |      | 10000 | ns   |       |
| MDIO Hold Time     | Thold        | 10   |      |       | ns   |       |
| MDIO Setup Time    | Tsetup       | 10   |      |       | ns   |       |
| GLB_ALM            | Tglb_alm_ass |      |      | 150   | ms   |       |
|                    | Tglb_alm_dea |      |      | 150   | ms   |       |

### OTU4 411-9D1F Operation Optical Characteristics

| Parameter   | Symbol          | Min.              | Typical | Max.    | Unit | Notes |
|---|-----------------|-------------------|---------|---------|------|-------|
| <b>Transmitter</b>  |                 |                   |         |         |      |       |
| Signaling Speed per Lane                                    | BRAVE           |                   | 27.95   |         | Gbps |       |
| Lane_0 Center Wavelength                                    | $\lambda_{C0}$  | 1294.53           | 1295.56 | 1296.59 | nm   |       |
| Lane_1 Center Wavelength                                    | $\lambda_{C1}$  | 1299.02           | 1300.05 | 1301.09 | nm   |       |
| Lane_2 Center Wavelength                                    | $\lambda_{C2}$  | 1303.54           | 1304.58 | 1305.63 | nm   |       |
| Lane_3 Center Wavelength                                    | $\lambda_{C3}$  | 1308.09           | 1309.14 | 1310.19 | nm   |       |
| Total Average Output Power                                  | PO1             | -                 |         | 8.9     | dBm  | 1, 2  |
| Average Launch Power per Lane                               | Peach1          | -2.5              |         | 2.9     | dBm  | 2     |
| Side Mode Suppression Ratio                                 | SMSR            | 30                |         |         | dB   |       |
| Optical Return Loss Tolerance                               |                 |                   |         | 20      | dB   |       |
| Extinction Ratio  | ER <sub>1</sub> | 7                 |         |         | dB   | 2     |
| Transmitter eye mask definition<br>{X1, X2, X3, Y1, Y2, Y3} |                 | G.959.1 Compliant |         |         |      | 2     |
| TX Disable Assert Time                                      | t_off           |                   |         | 100     | us   |       |
| <b>Receiver</b>   |                 |                   |         |         |      |       |
| Signaling Speed per Lane                                    | BRAVE           |                   | 27.95   |         | Gbps |       |
| Lane_0 Center Wavelength                                    | $\lambda_{C0}$  | 1294.53           | 1295.56 | 1296.59 | nm   |       |
| Lane_1 Center Wavelength                                    | $\lambda_{C1}$  | 1299.02           | 1300.05 | 1301.09 | nm   |       |
| Lane_2 Center Wavelength                                    | $\lambda_{C2}$  | 1303.54           | 1304.58 | 1305.63 | nm   |       |
| Lane_3 Center Wavelength                                    | $\lambda_{C3}$  | 1308.09           | 1309.14 | 1310.19 | nm   |       |
| Average Receive Power per Lane                              | Rpow1           | -8.8              |         | 4       | dBm  | 5     |
| Equivalent Sensitivity per Lane                             | Pmin1           |                   |         | -10.3   | dBm  | 7     |
| Receiver Overload per Lane                                  | Pmax            | 5.5               |         |         | dBm  |       |
| Optical Return Loss   | ORL             |                   |         | -26     | dB   |       |
| LOS Assert  | LOSA            | -21               |         |         | dBm  |       |
| LOS De-Assert   | LOSD            |                   |         | -11     | dBm  |       |
| LOS Hysteresis  |                 | 0.5               |         |         | dB   |       |

## 100GBASE-LR4 Operation Optical Characteristics

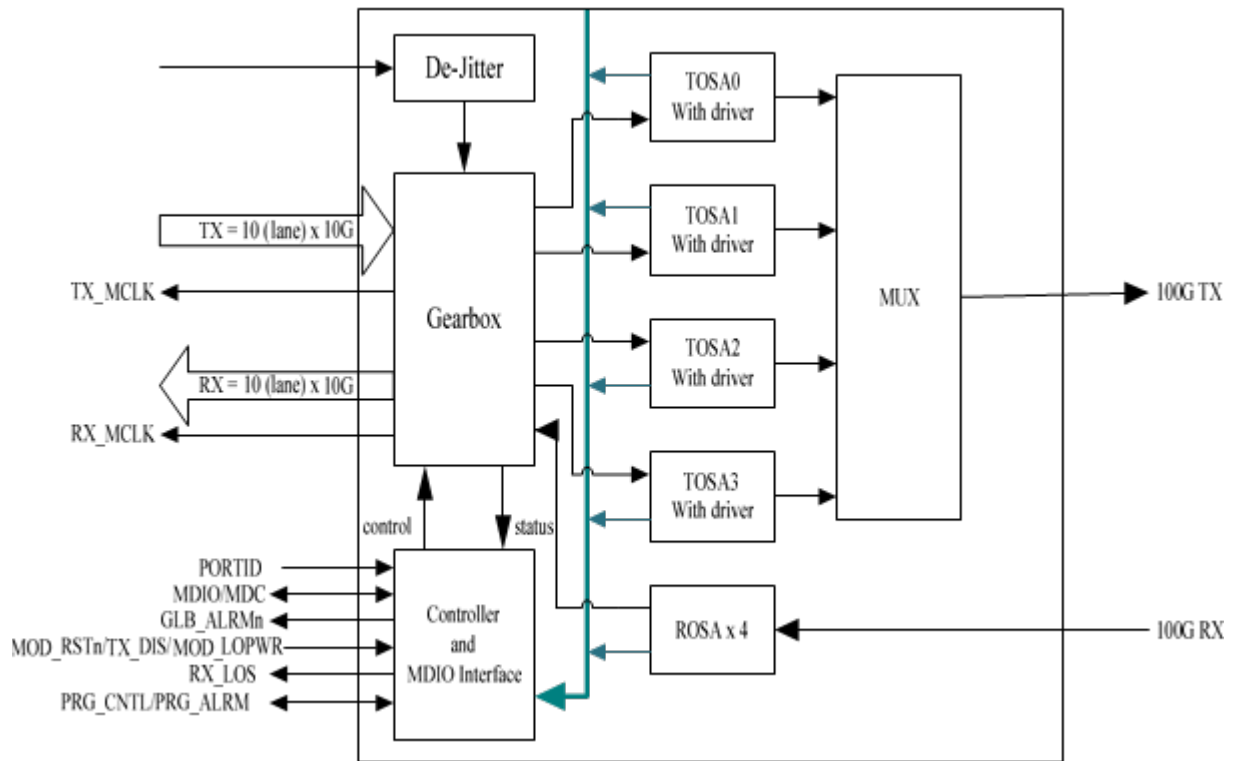
| Parameter   | Symbol             | Min.                       | Typical | Max.    | Unit | Notes |
|---|--------------------|----------------------------|---------|---------|------|-------|
| <b>Transmitter</b>  |                    |                            |         |         |      |       |
| Signaling Speed per Lane                                    | BRAVE              |                            | 25.78   |         | Gbps |       |
| Lane_0 Center Wavelength                                    | $\lambda_{C0}$     | 1294.53                    | 1295.56 | 1296.59 | nm   |       |
| Lane_1 Center Wavelength                                    | $\lambda_{C1}$     | 1299.02                    | 1300.05 | 1301.09 | nm   |       |
| Lane_2 Center Wavelength                                    | $\lambda_{C2}$     | 1303.54                    | 1304.58 | 1305.63 | nm   |       |
| Lane_3 Center Wavelength                                    | $\lambda_{C3}$     | 1308.09                    | 1309.14 | 1310.19 | nm   |       |
| Total Average Output Power                                  | PO2                | -                          |         | 10.5    | dBm  | 1, 4  |
| Average Launch Power per Lane                               | P <sub>each2</sub> | -4.3                       |         | 4.5     | dBm  | 4     |
| Side Mode Suppression Ratio                                 | SMSR               | 30                         |         |         | dB   |       |
| Optical Return Loss Tolerance                               |                    |                            |         | 20      | dB   |       |
| Extinction Ratio  | ER <sub>2</sub>    | 7                          |         |         | dB   | 4     |
| Transmitter eye mask definition<br>{X1, X2, X3, Y1, Y2, Y3} |                    | IEEE802.3ba-2010 Compliant |         |         |      | 4     |
| TX Disable Assert Time                                      | t <sub>off</sub>   |                            |         | 100     | us   |       |
| <b>Receiver</b>   |                    |                            |         |         |      |       |
| Signaling Speed per Lane                                    | BRAVE              |                            | 25.78   |         | Gbps |       |
| Lane_0 Center Wavelength                                    | $\lambda_{C0}$     | 1294.53                    | 1295.56 | 1296.59 | nm   |       |
| Lane_1 Center Wavelength                                    | $\lambda_{C1}$     | 1299.02                    | 1300.05 | 1301.09 | nm   |       |
| Lane_2 Center Wavelength                                    | $\lambda_{C2}$     | 1303.54                    | 1304.58 | 1305.63 | nm   |       |
| Lane_3 Center Wavelength                                    | $\lambda_{C3}$     | 1308.09                    | 1309.14 | 1310.19 | nm   |       |
| Average Receive Power per Lane                              | R <sub>pow2</sub>  | -10.6                      |         | 4.5     | dBm  | 6     |
| Receive Sensitivity (OMA) per Lane                          | P <sub>min2</sub>  |                            |         | -8.6    | dBm  | 8     |
| Stressed Sensitivity (OMA) per lane                         | SRS                |                            |         | -6.8    | dBm  |       |
| Receiver Overload per Lane                                  | P <sub>max</sub>   | 5.5                        |         |         | dBm  |       |
| Optical Return Loss   | ORL                |                            |         | -26     | dB   |       |
| LOS Assert  | LOSA               | -21                        |         |         | dBm  |       |
| LOS De-Assert   | LOSD               |                            |         | -11     | dBm  |       |
| LOS Hysteresis  |                    | 0.5                        |         |         | dB   |       |

### Notes:

1. Output is coupled into a 9/125 $\mu$ m single-mode fiber.
2. Filtered, measured with a PRBS 2<sup>31</sup>-1 test pattern @27.95Gbps
3. High speed I/O, internally AC coupled.
4. Filtered, measured with a PRBS 2<sup>31</sup>-1 test pattern @25.78Gbps
5. CFP transceiver works in OTU4 4I1-9D1F mode.
6. CFP transceiver works in 100GBASE-LR4 mode.

7. Minimum average optical power measured at BER less than 1E-12, with a  $2^{31}-1$  PRBS@27.95Gbps.
8. Minimum OMA optical power measured at BER less than 1E-12, with a  $2^{31}-1$  PRBS@25.78Gbps.

### Functional Description of Transceiver



### Electrical Pad Layout



## Pin Descriptions

### Part A: Bottom Row Pin Function Definition

| Pin | Name       | Function                   | Notes  |
|-----|------------|----------------------------|--|
| 1   | 3.3V_GND   | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground     |
| 2   | 3.3V_GND   | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground     |
| 3   | 3.3V_GND   | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground     |
| 4   | 3.3V_GND   | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground     |
| 5   | 3.3V_GND   | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground     |
| 6   | 3.3V       | 3.3V Module Supply Voltage | 3.3V ± 2.5%  |
| 7   | 3.3V       | 3.3V Module Supply Voltage | 3.3V ± 2.5%  |
| 8   | 3.3V       | 3.3V Module Supply Voltage | 3.3V ± 2.5%  |
| 9   | 3.3V       | 3.3V Module Supply Voltage | 3.3V ± 2.5%  |
| 10  | 3.3V       | 3.3V Module Supply Voltage | 3.3V ± 2.5%  |
| 11  | 3.3V       | 3.3V Module Supply Voltage | 3.3V ± 2.5%  |
| 12  | 3.3V       | 3.3V Module Supply Voltage | 3.3V ± 2.5%  |
| 13  | 3.3V       | 3.3V Module Supply Voltage | 3.3V ± 2.5%  |
| 14  | 3.3V       | 3.3V Module Supply Voltage | 3.3V ± 2.5%  |
| 15  | 3.3V       | 3.3V Module Supply Voltage | 3.3V ± 2.5%  |
| 16  | 3.3V_GND   | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground     |
| 17  | 3.3V_GND   | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground     |
| 18  | 3.3V_GND   | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground     |
| 19  | 3.3V_GND   | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground     |
| 20  | 3.3V_GND   | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground     |
| 21  | VND_IO_A   | I/O                        | Module Vendor I/O, NC  |
| 22  | VND_IO_B   | I/O                        | Module Vendor I/O, NC  |
| 23  | GND        | Ground                     | Signal Ground  |
| 24  | (TX_MCLKn) | Tx Monitor Clock O         | Tx Monitor Clock Output  |
| 25  | (TX_MCLKp) | Tx Monitor Clock O         | Tx Monitor Clock Output  |
| 26  | GND        | Ground                     | Signal Ground  |
| 27  | VND_IO_C   | I/O                        | Module Vendor I/O, must not connect at host board                    |
| 28  | VND_IO_D   | I/O                        | Module Vendor I/O, must not connect at host board                    |
| 29  | VND_IO_E   | I/O                        | Module Vendor I/O, must not connect at host board                    |
| 30  | PRG_CNTL1  | I                          | LVCOMS   |
| 31  | PRG_CNTL2  | I                          | LVCOMS   |
| 32  | PRG_CNTL3  | I                          | LVCOMS   |
| 33  | PRG_ALARM1 | O                          | LVCOMS   |
| 34  | PRG_ALARM2 | O                          | LVCOMS   |
| 35  | PRG_ALARM3 | O                          | LVCOMS   |
| 36  | TX_DIS     | Transmitter Disable I      | "1" or NC = transmitter disabled,<br>"0" = transmitter enabled       |
| 37  | MOD_LOPW R | Module Low Power Mode I    | "1" or NC: module in low power (safe) mode,<br>"0": power-on enabled |
| 38  | MOD_ABS    | Module Absent O            | "1" or NC: module absent,<br>"0": module present                     |
| 39  | MOD_RSTn   | Module Reset I             | "0" resets the module,<br>"1" or NC = module enabled                 |
| 40  | RX_LOS     | Loss of Signal O           | "1": low optical signal, "0": normal condition                       |

|    |           |                            |   |
|----|-----------|----------------------------|---|
| 41 | GLB_ALRMn | Global Alarm O             | "0": alarm condition in any MDIO Alarm register,<br>"1": no alarm condition |
| 42 | PRTADR4   | 1.2V CMOS I                | MDIO Physical Port address bit4   |
| 43 | PRTADR3   | 1.2V CMOS I                | MDIO Physical Port address bit3   |
| 44 | PRTADR2   | 1.2V CMOS I                | MDIO Physical Port address bit2   |
| 45 | PRTADR1   | 1.2V CMOS I                | MDIO Physical Port address bit1   |
| 46 | PRTADR0   | 1.2V CMOS I                | MDIO Physical Port address bit0   |
| 47 | MDIO      | 1.2V CMOS I/O              | Management Data I/O bi-directional data                                     |
| 48 | MDC       | 1.2V CMOS I                | Management Data Clock   |
| 49 | GND       | Ground                     | Signal Ground   |
| 50 | VND_IO_F  | I/O                        | Module Vendor I/O, Not Connected Internally                                 |
| 51 | VND_IO_G  | I/O                        | Module Vendor I/O, Not Connected Internally                                 |
| 52 | GND       | Ground                     | Signal Ground   |
| 53 | VND_IO_H  | I/O                        | Module Vendor I/O, Not Connected Internally                                 |
| 54 | VND_IO_J  | I/O                        | Module Vendor I/O, Not Connected Internally                                 |
| 55 | 3.3V_GND  | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground            |
| 56 | 3.3V_GND  | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground            |
| 57 | 3.3V_GND  | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground            |
| 58 | 3.3V_GND  | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground            |
| 59 | 3.3V_GND  | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground            |
| 60 | 3.3V      | 3.3V Module Supply Voltage | 3.3V ± 2.5%   |
| 61 | 3.3V      | 3.3V Module Supply Voltage | 3.3V ± 2.5%   |
| 62 | 3.3V      | 3.3V Module Supply Voltage | 3.3V ± 2.5%   |
| 63 | 3.3V      | 3.3V Module Supply Voltage | 3.3V ± 2.5%   |
| 64 | 3.3V      | 3.3V Module Supply Voltage | 3.3V ± 2.5%   |
| 65 | 3.3V      | 3.3V Module Supply Voltage | 3.3V ± 2.5%   |
| 66 | 3.3V      | 3.3V Module Supply Voltage | 3.3V ± 2.5%   |
| 67 | 3.3V      | 3.3V Module Supply Voltage | 3.3V ± 2.5%   |
| 68 | 3.3V      | 3.3V Module Supply Voltage | 3.3V ± 2.5%   |
| 69 | 3.3V      | 3.3V Module Supply Voltage | 3.3V ± 2.5%   |
| 70 | 3.3V_GND  | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground            |
| 71 | 3.3V_GND  | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground            |
| 72 | 3.3V_GND  | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground            |
| 73 | 3.3V_GND  | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground            |
| 74 | 3.3V_GND  | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground            |

#### Part B: Top Row Pin Function Definition

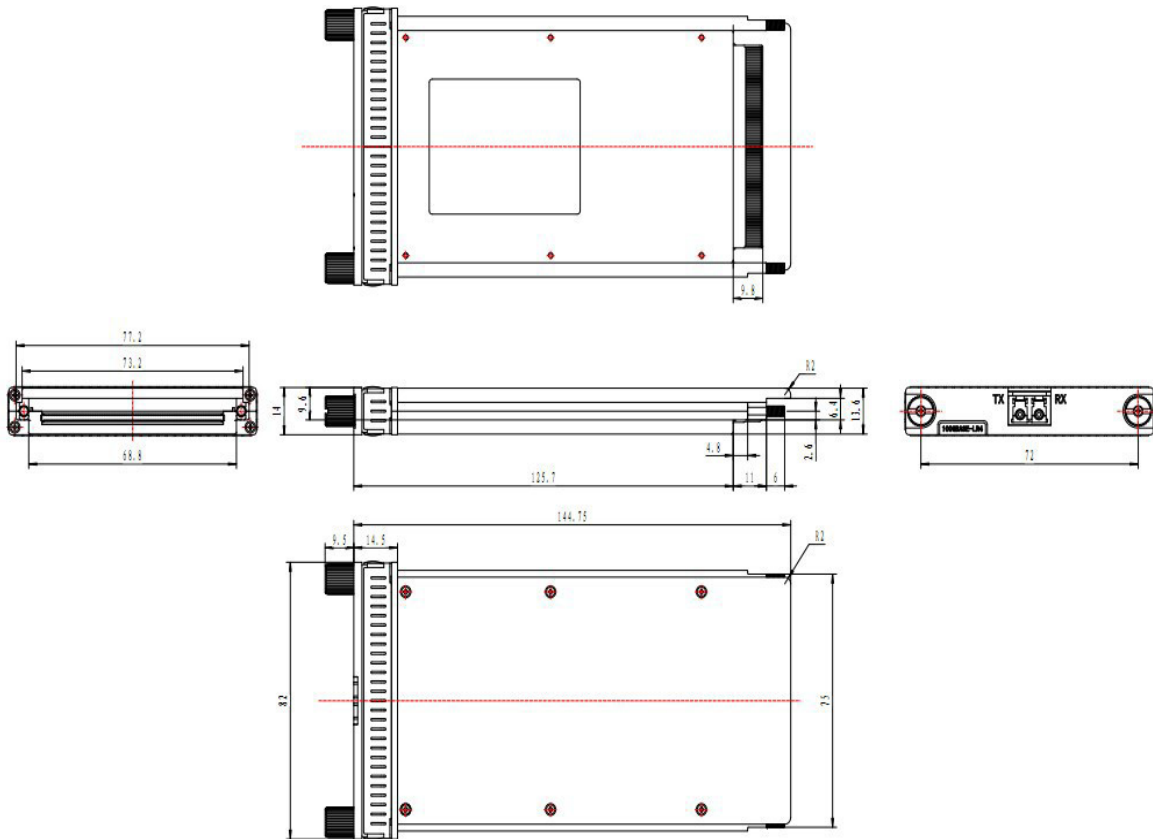
| Pin | Name    | Function          | Notes  |
|-----|---------|-------------------|--|
| 148 | GND     | Ground            | Signal Ground  |
| 147 | REFCLKn | Reference Clock I | Reference Clock Input  |
| 146 | REFCLKp | Ground            | 3.3V Module Supply Ground, Internally connected to Signal Ground |
| 145 | GND     | Ground            | Signal Ground  |
| 144 | N.C.    |                   | Not Connected Internally   |
| 143 | N.C.    |                   | Not Connected Internally   |
| 142 | GND     | Ground            | Signal Ground  |
| 141 | TX9n    | Lane 9 Tx Input I |  |

|     |      |                    |                          |
|-----|------|--------------------|--------------------------|
| 140 | TX9p | Lane 9 Tx Input I  |                          |
| 139 | GND  | Ground             | Signal Ground            |
| 138 | TX8n | Lane 8 Tx Input I  | 3.3V ± 2.5%              |
| 137 | TX8p | Lane 8 Tx Input I  | 3.3V ± 2.5%              |
| 136 | GND  | Ground             | Signal Ground            |
| 135 | TX7n | Lane 7 Tx Input I  | 3.3V ± 2.5%              |
| 134 | TX7p | Lane 7 Tx Input I  | 3.3V ± 2.5%              |
| 133 | GND  | Ground             | Signal Ground            |
| 132 | TX6n | Lane 6 Tx Input I  |                          |
| 131 | TX6p | Lane 6 Tx Input I  |                          |
| 130 | GND  | Ground             | Signal Ground            |
| 129 | TX5n | Lane 5 Tx Input I  |                          |
| 128 | TX5p | Lane 5 Tx Input I  |                          |
| 127 | GND  | Ground             | Signal Ground            |
| 126 | TX4n | Lane 4 Tx Input I  |                          |
| 125 | TX4p | Lane 4 Tx Input I  |                          |
| 124 | GND  | Ground             | Signal Ground            |
| 123 | TX3n | Lane 3 Tx Input I  |                          |
| 122 | TX3p | Lane 3 Tx Input I  |                          |
| 121 | GND  | Ground             | Signal Ground            |
| 120 | TX2n | Lane 2 Tx Input I  |                          |
| 119 | TX2p | Lane 2 Tx Input I  |                          |
| 118 | GND  | Ground             | Signal Ground            |
| 117 | TX1n | Lane 1 Tx Input I  |                          |
| 116 | TX1p | Lane 1 Tx Input I  |                          |
| 115 | GND  | Ground             | Signal Ground            |
| 114 | TX0n | Lane 0 Tx Input I  |                          |
| 113 | TX0p | Lane 0 Tx Input I  |                          |
| 112 | GND  | Ground             | Signal Ground            |
| 111 | GND  | Ground             | Signal Ground            |
| 110 | N.C. |                    | Not Connected Internally |
| 109 | N.C. |                    | Not Connected Internally |
| 108 | GND  | Ground             | Signal Ground            |
| 107 | RX9n | Lane 9 Rx Output O |                          |
| 106 | RX9p | Lane 9 Rx Output O |                          |
| 105 | GND  | Ground             | Signal Ground            |
| 104 | RX8n | Lane 8 Rx Output O |                          |
| 103 | RX8p | Lane 8 Rx Output O |                          |
| 102 | GND  | Ground             | Signal Ground            |
| 101 | RX7n | Lane 7 Rx Output O |                          |
| 100 | RX7p | Lane 7 Rx Output O |                          |
| 99  | GND  | Ground             | Signal Ground            |
| 98  | RX6n | Lane 6 Rx Output O |                          |
| 97  | RX6p | Lane 6 Rx Output O |                          |
| 96  | GND  | Ground             | Signal Ground            |
| 95  | RX5n | Lane 5 Rx Output O |                          |
| 94  | RX5p | Lane 5 Rx Output O |                          |

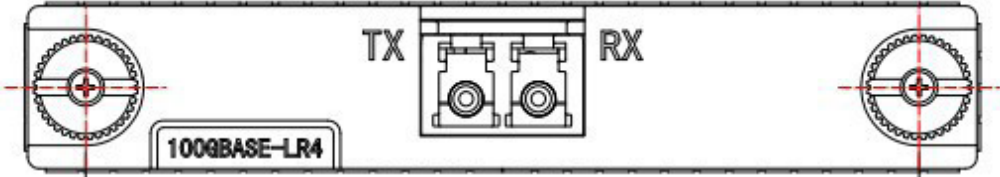


|    |          |                    |                         |
|----|----------|--------------------|-------------------------|
| 93 | GND      | Ground             | Signal Ground           |
| 92 | RX4n     | Lane 4 Rx Output O |                         |
| 91 | RX4p     | Lane 4 Rx Output O |                         |
| 90 | GND      | Ground             | Signal Ground           |
| 89 | RX3n     | Lane 3 Rx Output O |                         |
| 88 | RX3p     | Lane 3 Rx Output O |                         |
| 87 | GND      | Ground             | Signal Ground           |
| 86 | RX2n     | Lane 2 Rx Output O |                         |
| 85 | RX2p     | Lane 2 Rx Output O |                         |
| 84 | GND      | Ground             | Signal Ground           |
| 83 | RX1n     | Lane 1 Rx Output O |                         |
| 82 | RX1p     | Lane 1 Rx Output O |                         |
| 81 | GND      | Ground             | Signal Ground           |
| 80 | RX0n     | Lane 0 Rx Output O |                         |
| 79 | RX0p     | Lane 0 Rx Output O |                         |
| 78 | GND      | Ground             | Signal Ground           |
| 77 | RX_MCLKn | Rx Monitor Clock O | Rx Monitor Clock Output |
| 76 | RX_MCLKp | Rx Monitor Clock O | Rx Monitor Clock Output |
| 75 | GND      | Ground             | Signal Ground           |

### Mechanical Specifications



Laser Emission



## About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is engrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications from ranging from NEBS Level 3 to ISO 9001:2005 with every new development while maintaining the signature reliability of its products.



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