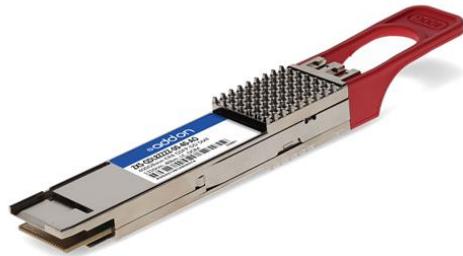


## ZXS-QDL8ZZZZ-00-40-AO

Infinera® ZXS-QDL8ZZZZ-00-40 Compatible TAA 400GBase-ER8 QSFP-DD Transceiver (SMF, 1270nm to 1330nm, 40km, LC, DOM, 0 to 70C)

### Features

- Hot-pluggable QSFP-DD Type 2 form factor
- Power dissipation < 13W
- Supports 425Gb/s aggregate bit rate
- Single-mode Fiber
- Aligned with IEEE 802.3bs
- Single 3.3V power supply
- Operating case temperature: 0C to +70C



### Applications

- 400GBase Ethernet
- Access and Enterprise

### Product Description

This Infinera® ZXS-QDL8ZZZZ-00-40 compatible QSFP-DD transceiver provides 400GBase-ER8 throughput up to 40km over single-mode fiber (SMF) using a wavelength of 1270nm to 1330nm via an LC connector. It is guaranteed to be 100% compatible with the equivalent Infinera® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."



## Regulatory Compliance

- ESD to the Electrical PINs: compatible with MIL-STD-883E Method 3015.4
- ESD to the LC Receptacle: compatible with IEC 61000-4-3
- EMI/EMC compatible with FCC Part 15 Subpart B Rules, EN55022:2010
- Laser Eye Safety compatible with FDA 21CFR, EN60950-1& EN (IEC) 60825-1,2
- RoHS compliant with EU RoHS 2.0 directive 2015/863/EU

## Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Power Supply Voltage	VCC	-0.5	4.0	V	
Storage Temperature	Ts	-40	+85	°C	
Case Operating Temperature	Top	0	+70	°C	
Relative Humidity (non-condensing)	RH	15	85	%	
Receiver Damage Threshold, per Lane	P <sub>Rdmg</sub>	6.3		dBm	
Bit Rate (all wavelengths combined)	BR		425	Gb/s	1
Bit Error Ratio	BER		2.4x10 <sup>-4</sup>		2
<b>Maximum Supported Distances</b>					
Fiber Type					
SMF per G.652	Lmax1		10	km	

## Notes:

1. Supports 400GBASE-LR8 per IEEE P802.3bs.
2. As defined by IEEE P802.3bs.

**Electrical Characteristics (EOL,  $T_{OP} = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.135$  to  $3.465$  Volts)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
<b>Supply Voltage</b>	V <sub>CC</sub>	3.135	3.3	3.465	V	
<b>Supply Current</b>	I <sub>CC</sub>			3.83	A	
<b>Module total power</b>	P			13	W	1
<b>Transmitter</b>						
<b>Signaling Rate, each Lane</b>	V <sub>IN, pp, diff</sub>	$26.5625 \pm 100$ ppm			GBd	
<b>Differential data input voltage per lane</b>	TP1a	900			mVpp	1
<b>Differential input return loss</b>		Per equation (83E-5) IEEE802.3bm			dB	
<b>Differential to common mode input return loss</b>		Per equation (83E-6) IEEE802.3bm			dB	
<b>Differential termination mismatch</b>				10	%	
<b>Module stress input test</b>		Per 120E.3.4.1 IEEE802.3bs				3
<b>Single-ended voltage tolerance range</b>		-0.4		3.3	V	
<b>DC common mode voltage</b>		-350		2850	mV	4
<b>Receiver</b>						
<b>Signaling Rate, each lane</b>		$26.5625 \pm 100$ ppm			GBd	
<b>AC common-mode output voltage (RMS)</b>				17.5	mV	
<b>Differential output voltage</b>				900	mV	
<b>Near-end ESMW (Eye symmetry mask width)</b>		0.265			UI	
<b>Near-end Eye height, differential (min)</b>		70			mV	
<b>Far-end ESMW (Eye symmetry mask width)</b>		0.2			UI	
<b>Far-end Eye height, differential (min)</b>		30			mV	
<b>Far-end pre-cursor ISI ratio</b>		-4.5		2.5	dB	
<b>Differential output return loss</b>		Per equation 83E-2 IEEE802.3bm				
<b>Common to differential mode conversion return loss</b>		Per equation 83E-3 IEEE802.3bm				
<b>Differential termination mismatch</b>				10	%	
<b>Transition time (min, 20% to 80%)</b>		9.5			ps	
<b>DC common mode voltage (min)</b>		-350		2850	mV	4

**Notes:**

1. Maximum total power value is specified across the full temperature and voltage range.
2. With the exception to 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
3. Meets specified BER
4. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

**Optical Characteristics (EOL,  $T_{OP} = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.135$  to  $3.465$  Volts)**

Meets 400GBASE-LR8 as being defined by IEEE P802.3bs

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
<b>Transmitter</b>						
Signaling rate (each lane (range))		$26.5625 \pm 100$ ppm			GBd	
Modulation Format		PAM4				
Lane wavelengths (range)		1272.55 to 1274.54 1276.89 to 1278.89 1281.25 to 1283.27 1285.65 to 1287.68 1294.53 to 1296.59 1299.02 to 1301.09 1303.54 to 1305.63 1308.09 to 1310.19			nm	
Side-mode suppression ratio (SMSR)		30			dB	
Total average launch power				13.2	dBm	
Average launch power, each lane				5.3	dBm	1
Average launch power, each lane		-2.8			dBm	2
Outer Optical Modulation Amplitude (OMAouter), each lane		0.2		5.7	dBm	3
Difference in launch power between any two lanes (OMAouter)				4	dB	
Launch power in OMAouter minus TDECQ, each lane		-1.1			dBm	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane				3.3	dB	
Average launch power of OFF transmitter, each lane				-30	dBm	
Extinction ratio		3.5			dB	
RIN <sub>15.1</sub> OMA				-132	dB/Hz	
Optical return loss tolerance				15.1	dB	
Transmitter reflectance				-26	dB	4
<b>Receiver</b>						
Signaling rate (each lane (range))		$26.5625 \pm 100$ ppm			GBd	
Modulation Format		PAM4				
Lane wavelengths (range)		1272.55 to 1274.54 1276.89 to 1278.89 1281.25 to 1283.27 1285.65 to 1287.68 1294.53 to 1296.59 1299.02 to 1301.09 1303.54 to 1305.63 1308.09 to 1310.19			nm	
Damage threshold, each lane		6.3			dBm	5
Average receive power, each lane				5.3	dBm	
Average receive power, each lane		-9.1			dBm	6
Receive power (OMAouter), each lane				5.7	dBm	

<b>Difference in receive power between any two lanes (OMAouter)</b>				4.5	dBm	
<b>Receiver reflectance</b>				-26	dB	
<b>Receiver sensitivity (OMAouter), each lane</b>				-7.1	dBm	7
<b>Stressed receiver sensitivity (OMAouter), each lane</b>				-4.7	dBm	8
<b>Conditions for Stress Receiver Sensitivity Test</b>						
<b>Stressed eye closure for PAM4 (SECQ), lane under test</b>		3.3			dB	9
<b>OMAouter of each aggressor lane</b>		-0.2			dBm	9

**Notes:**

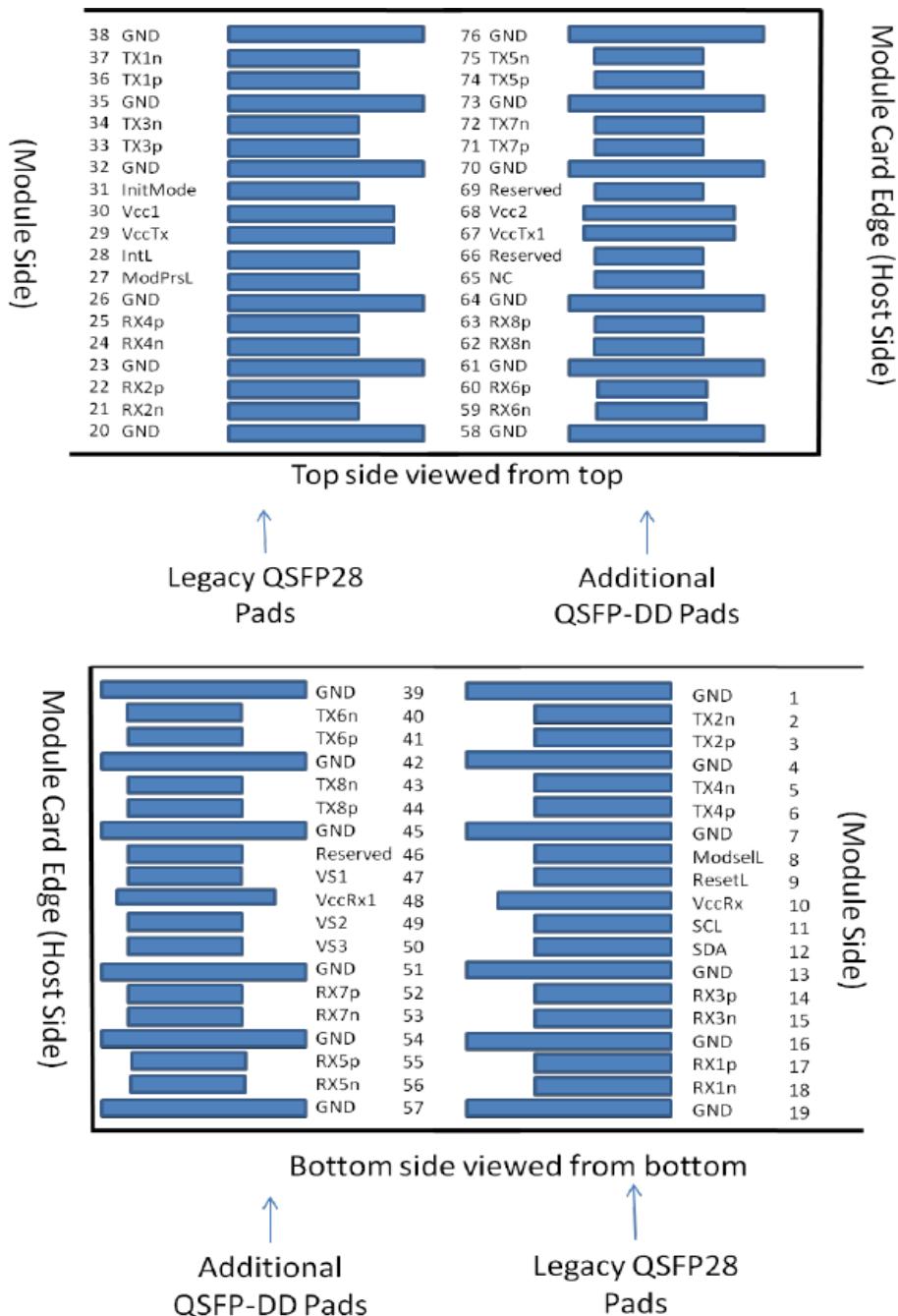
1. As the total average launch power limit has to be met, not all of the lanes can operate at the maximum average launch power, each lane.
2. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
3. Even if the TDECQ < 1 dB, the OMAouter (min) must exceed this value
4. Transmitter reflectance is defined looking into the transmitter
5. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
6. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
7. Receiver sensitivity (OMAouter), each lane (max) is informative.
8. Measured with conformance test signal at TP3 (see 122.8.9) for the BER specified in 122.1.1.
9. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

## Pin Descriptions

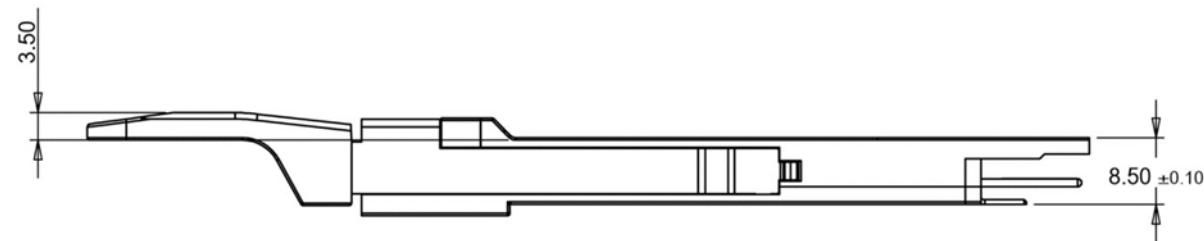
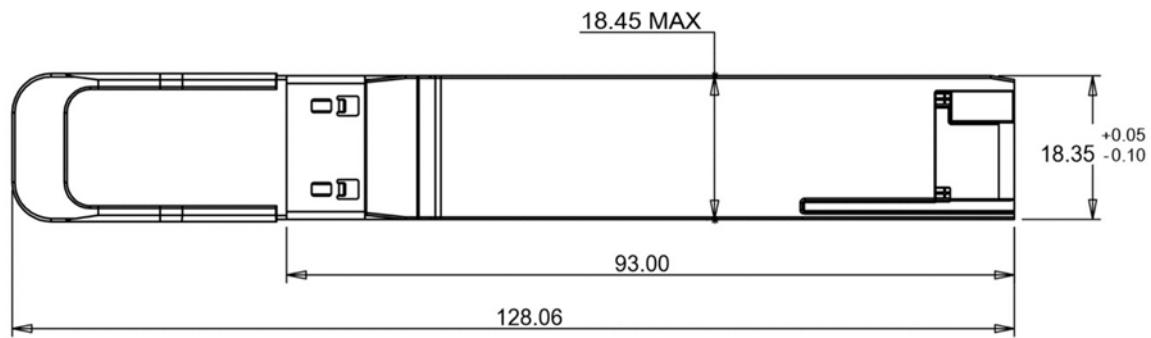
Pin	Logic	Symbol	Name/Descriptions	Plug Sequence
1		GND	Ground	1B
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B
4		GND	Ground	1B
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B
7		GND	Ground	1B
8	LVTTL-I	ModSelL	Module Select	3B
9	LVTTL-I	ResetL	Module Reset	3B
10		VccRx	+3.3V Power Supply Receiver	2B
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B
13		GND	Ground	1B
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B
15	CML-O	Rx3n	Receiver Inverted Data Output	3B
16	GND	Ground	1B	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B
18	CML-O	Rx1n	Receiver Inverted Data Output	3B
19		GND	Ground	1B
20		GND	Ground	1B
21	CML-O	Rx2n	Receiver Inverted Data Output	3B
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B
23		GND	Ground	1B
24	CML-O	Rx4n	Receiver Inverted Data Output	3B
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B
26		GND	Ground	1B
27	LVTTL-O	ModPrsL	Module Present	3B
28	LVTTL-O	IntL	Interrupt	3B
29		VccTx	+3.3V Power supply transmitter	2B
30		Vcc1	+3.3V Power supply	2B
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B
32		GND	Ground	1B
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B
35		GND	Ground	1B
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B
38		GND	Ground	1B
39		GND	Ground	1A
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A

<b>41</b>	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A
<b>42</b>		GND	Ground	1A
<b>43</b>	CML-I	Tx8n	Transmitter Inverted Data Input	3A
<b>44</b>	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A
<b>45</b>		GND	Ground	1A
<b>46</b>		Reserved	For future use	3A
<b>47</b>		VS1	Module Vendor Specific 1	3A
<b>48</b>		VccRx1	3.3V Power Supply	2A
<b>49</b>		VS2	Module Vendor Specific 2	3A
<b>50</b>		VS3	Module Vendor Specific 3	3A
<b>51</b>		GND	Ground	1A
<b>52</b>	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A
<b>53</b>	CML-O	Rx7n	Receiver Inverted Data Output	3A
<b>54</b>		GND	Ground	1A
<b>55</b>	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A
<b>56</b>	CML-O	Rx5n	Receiver Inverted Data Output	3A
<b>57</b>		GND	Ground	1A
<b>58</b>		GND	Ground	1A
<b>59</b>	CML-O	Rx6n	Receiver Inverted Data Output	3A
<b>60</b>	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A
<b>61</b>		GND	Ground	1A
<b>62</b>	CML-O	Rx8n	Receiver Inverted Data Output	3A
<b>63</b>	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A
<b>67</b>		GND	Ground	1A
<b>68</b>		NC	No Connect	3A
<b>69</b>		Reserved	For future use	3A
<b>70</b>		VccTx1	3.3V Power Supply	2A
<b>71</b>		Vcc2	3.3V Power Supply	2A
<b>72</b>		Reserved	For Future Use	3A
<b>73</b>		GND	Ground	1A
<b>74</b>	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A
<b>75</b>	CML-I	Tx7n	Transmitter Inverted Data Input	3A
<b>76</b>		GND	Ground	1A

## MSA Compliant Connector



## Mechanical Specifications



## **About AddOn Networks**

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is engrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications from ranging from NEBS Level 3 to ISO 9001:2005 with every new development while maintaining the signature reliability of its products.

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