QSFPDD-8SFP56-PDAC1M-AO

MSA and TAA Compliant 400GBase-CU QSFP-DD 400G to 8xSFP56 Direct Attach Cable (Passive Twinax, 1m)

Features



- Compliant with QSFP-DD MSA Specification Rev 3.4
- SFF-8679 electrical interface compliant
- SFF-8636 management interface support
- Compliant with IEEE802.3Bj, By, IEEE802.3CD Standard
- Support 28 Gbps NRZ or 56 Gbps PAM-4 electrical data rates/channel
- I2C for EEPROM communication
- Pull to Release latch design
- Excellent EMI/EMC performance 360-degree cable shield termination
- Advantage dual side pre-solder automated assembly technologies
- Low loss, stronger mechanical features, more flexible
- ROHS-6 Compliant

Applications

- Servers
- Switches
- Routers
- Data Centers
- High Performance Computing

Product Description

This is an MSA compliant 400GBase-CU QSFP-DD to 8xSFP56 direct attach cable that operates over passive copper with a maximum reach of 1.0m (3.3ft). It has been programmed, uniquely serialized, and data-traffic and application tested to ensure it is 100% compliant and functional. Our direct attach cables are built to complywith MSA (Multi-Source Agreement) standards. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's direct attach cables are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."

Order Information

Part Number	Description
QSFPDD-8SFP56-PDAC1M-AO	MSA and TAA Compliant 400GBase-CU QSFP-DD 400G to 8xSFP56 Direct Attach Cable (Passive Twinax, 1m)

Regulatory Compliance

Certification	Standard
Laser Eye Safety	IEC: 60825-1, 3rd Edition FDA: CFR-21 Sections 1040.10 and 1040.11
Product Safety	TUV: EN62368-1 UL/CSA 60950-1
EMC/EMI	FCC: Part 15 sb.B EN: 55032/55024

Mechanical Characteristics

Length	Wire Gauge	Cable OD	Cable Jacket Material	Flammability Rating
1m	32 AWG	3.81mm	PVC	VW-1

Electrical Characteristics

Parameter	Specification
Impedance	100 ohm
Data Rate	56Gbps per lane (PAM4)
Voltage	3.3V DC
Current (signal application only)	0.75A
Operating Temperature	-10°C to +60°C
High Speed Compliant	IEEE 802.3cd

QSFP-DD to 8xSFP56 Wiring Schematic

P1 (QSFP-DD)			P2 (SFP56)	
GND				GND
TX1+	36	⟷	13	RX1+
TX1-	37	⟷	12	RX1-
GND				GND
RX1+	17	⟷	18	TX1+
RX1-	18	⟷	19	TX1-
GND				GND

P1 (QSFP-DD)			P3 (SFP56)	
GND				GND
TX2+	3	⟷	13	RX1+
TX2-	2	⟷	12	RX1-
GND				GND
RX2+	22	⟷	18	TX1+
RX2-	21	⟷	19	TX1-
GND				GND

P1 (QSFP-DD)			P4 (SFP56)	
GND				GND
TX3+	33	⟷	13	RX1+
TX3-	34	⟷	12	RX1-
GND				GND
RX3+	14	⟷	18	TX1+
RX3-	15	⟷	19	TX1-
GND				GND

P1 (QSFP-DD)			P5 (SFP56)	
GND				GND
TX4+	6	⟷	13	RX1+
TX4-	5	⟷	12	RX1-
GND				GND
RX4+	25	⟷	18	TX1+
RX4-	24	⟷	19	TX1-
GND				GND

P1 (QSFP-DD)			P6 (SFP56)	
GND				GND
TX5+	74	⟷	13	RX1+
TX5-	75	⟷	12	RX1-
GND				GND
RX5+	55	⟷	18	TX1+
RX5-	56	⟷	19	TX1-
GND				GND

P1 (QSFP-DD)			P7 (SFP56)	
GND				GND
TX6+	41	⟷	13	RX1+
TX6-	40	⟷	12	RX1-
GND				GND
RX6+	60	⟷	18	TX1+
RX6-	59	⟷	19	TX1-
GND				GND

P1 (QSFP-DD)			P8 (SFP56)	
GND				GND
TX7+	71	⟷	13	RX1+
TX7-	72	⟷	12	RX1-
GND				GND
RX7+	52	⟷	18	TX1+
RX7-	53	⟷	19	TX1-
GND				GND

P1 (QSFP-DD)			P9 (SFP56)	
GND				GND
TX8+	44	⟷	13	RX1+
TX8-	43	⟷	12	RX1-
GND				GND
RX8+	63	⟷	18	TX1+
RX8-	62	⟷	19	TX1-
GND				GND

QSFP-DD Pin Descriptions

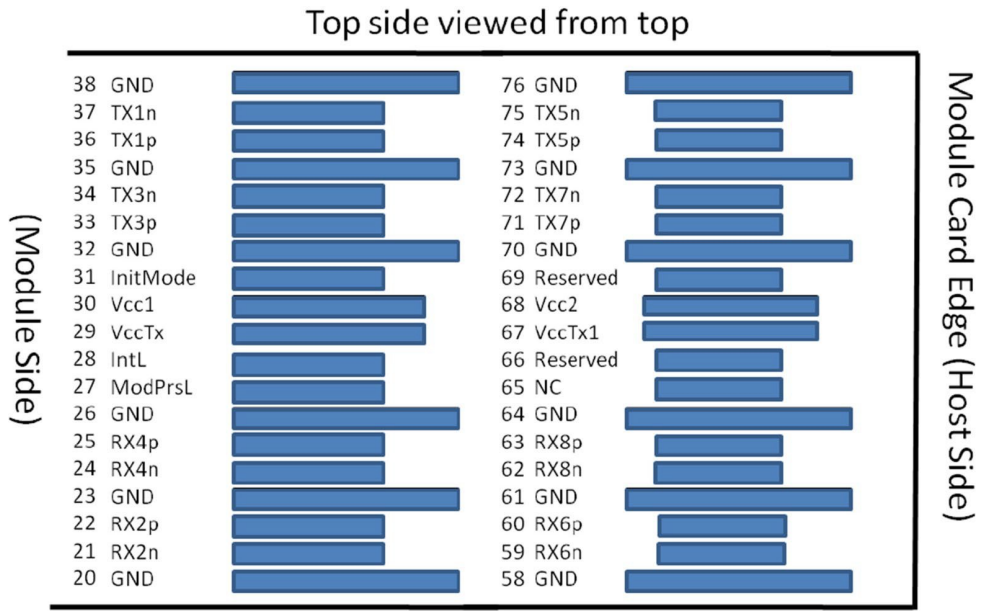
PIN	Logic	Symbol	Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	
12	LVCMOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vccl	+3.3V Power Supply	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1

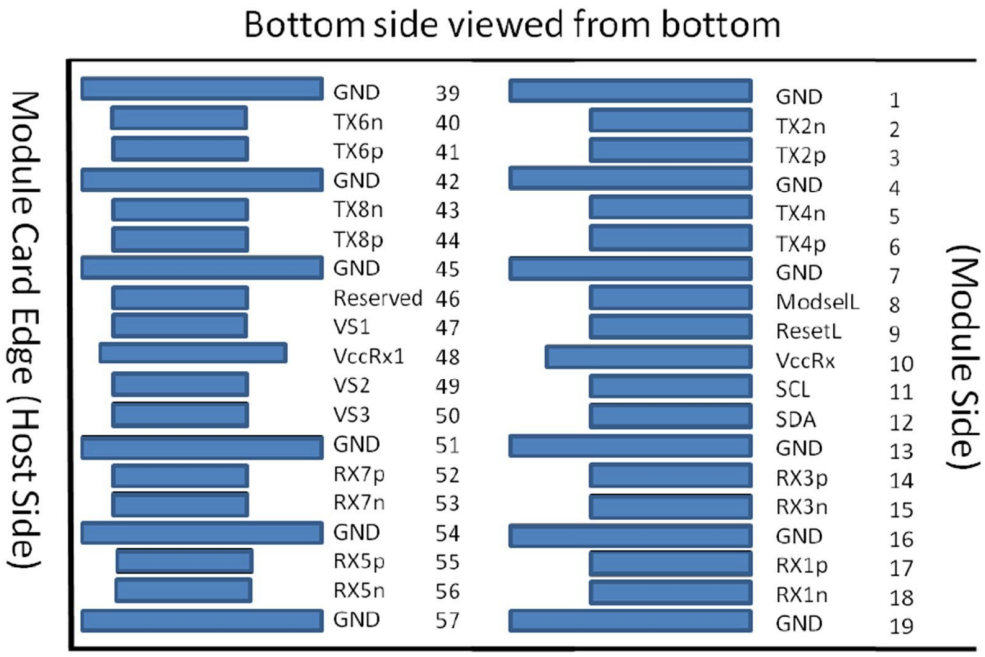
PIN		Symbol	Description	Notes
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	3
47		VSl	Module Vendor Specific 1	3
48		VccRx1	3.3V Power Supply	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69		Reserved	For future use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

Notes:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

QSFP-DD Electrical Pin-out Details



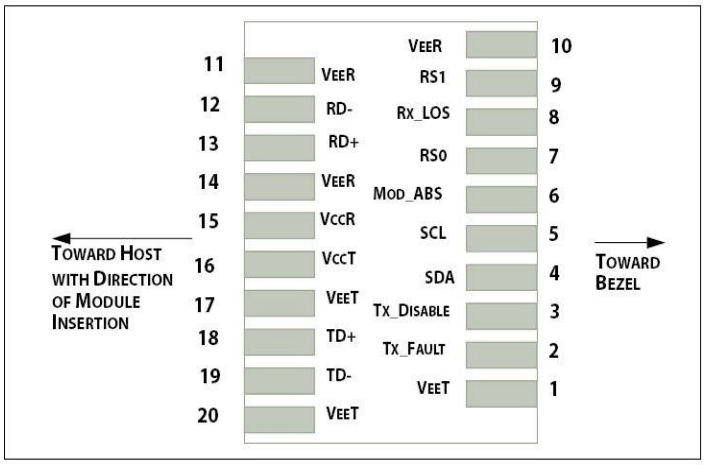

Bottom side viewed from bottom
Module Card Edge (Host Side)
(Module Side)
GND 39
TX6n 40
TX6p 41
GND 42
TX8n 43
TX8p 44
GND 45
Reserved 46
VS1 47
VccRx1 48
VS2 49
VS3 50
GND 51
RX7p 52
RX7n 53
GND 54
RX5p 55
RX5n 56
GND 57
GND 1
TX2n 2
TX2p 3
GND 4
TX4n 5
TX4p 6
GND 7
ModselL 8
ResetL 9
VccRx 10
SCL 11
SDA 12
GND 13
RX3p 14
RX3n 15
GND 16
RX1p 17
RX1n 18
GND 19

SFP56 Pin Definitions

Pin	Symbol	Name/Descriptions	Notes
1	VeeT	Transmitter Ground	1
2	TX_Fault	Transmitter Fault (LVTTL-O) - High indicates a fault condition	2
3	TX_Disable	Transmitter Disable (LVTTL-I) – High or open disables the transmitter	3
4	SDA	Two wire serial interface Data Line (LVCMOS-I/O) (MOD-DEF2)	4
5	SCL	Two wire serial interface Clock Line (LVCMOS-I/O) (MOD-DEF1)	4
6	MOD_ABS	Module Absent (Output), connected to VeeT or VeeR in the module	5
7	RS0	NA	6
8	RX_LOS	Receiver Loss of Signal (LVTTL-O)	2
9	RS1	NA	6
10	VeeR	Receiver Ground	1
11	VeeR	Receiver Ground	1
12	RD-	Inverse Received Data out (CML-O)	
13	RD+	Received Data out (CML-O)	
14	VeeR	Receiver Ground	
15	VccR	Receiver Power - +3.3V	
16	VccT	Transmitter Power - +3.3 V	
17	VeeT	Transmitter Ground	1
18	TD+	Transmitter Data In (CML-I)	
19	TD-	Inverse Transmitter Data In (CML-I)	
20	VeeT	Transmitter Ground	1

Notes:

1. The module signal grounds are isolated from the module case.
2. This is an open collector/drain output that on the host board requires a 4.7KΩ to 10KΩ pull-up resistor to Vcc-Host.
3. This input is internally biased high with a 4.7KΩ to 10KΩ pull-up resistor to VccT.
4. Two-Wire Serial interface clock and data lines require an external pull-up resistor.
5. This is a ground return that on the host board requires a 4.7KΩ to 10KΩ pull-up resistor to Vcc-Host.
6. Rate select not available

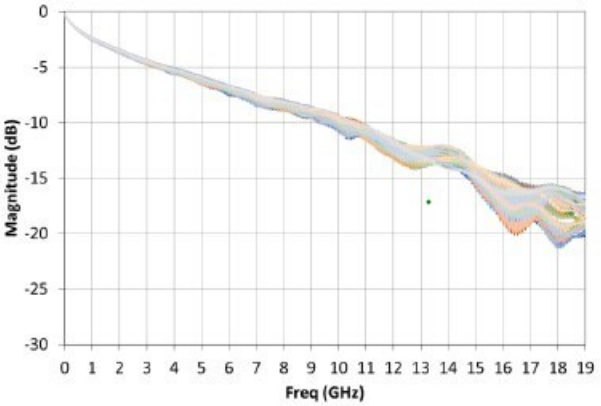


Host PCB SFP56 Pad Assignment Top View

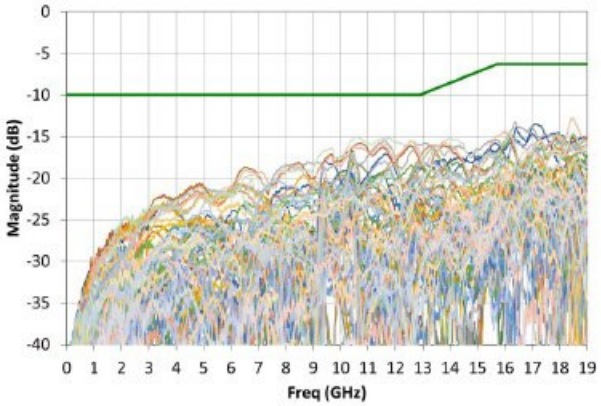
SI Test Reports

1m 30 AWG

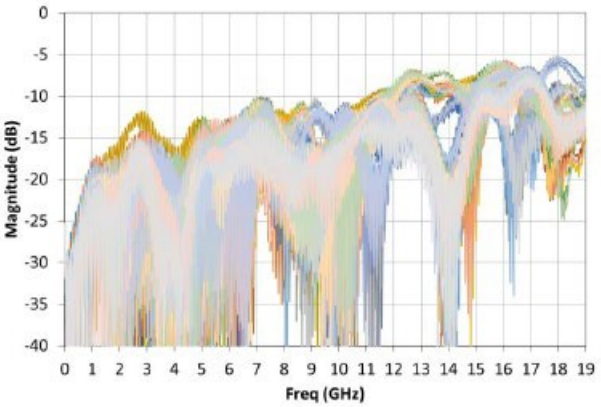
SDD21



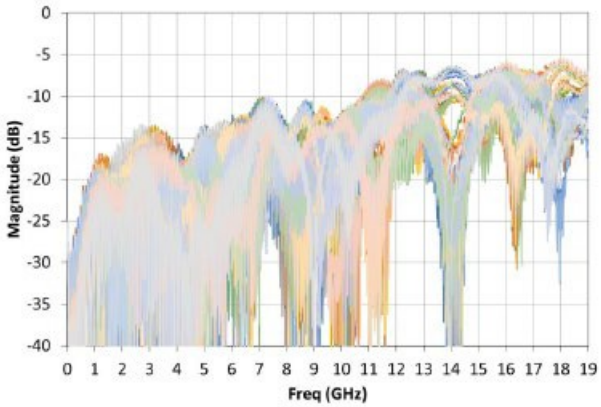
SCD21 – SDD21



SDD11



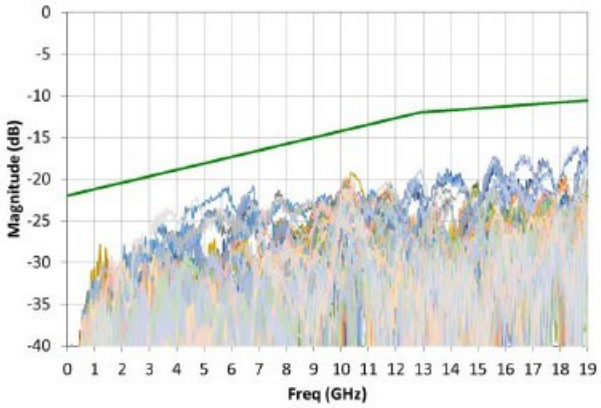
SDD22



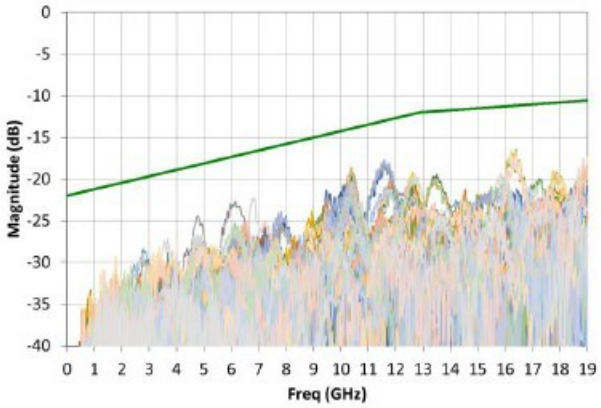
Worst ERL11 (target>11dB)	Worst ERL22 (target>11dB)
17.6dB	17.5dB

1m 30AWG

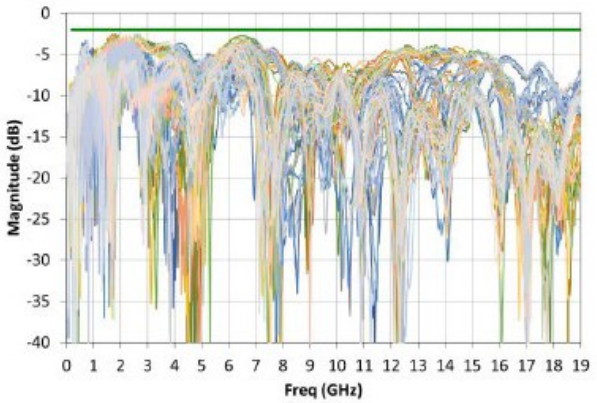
SCD11



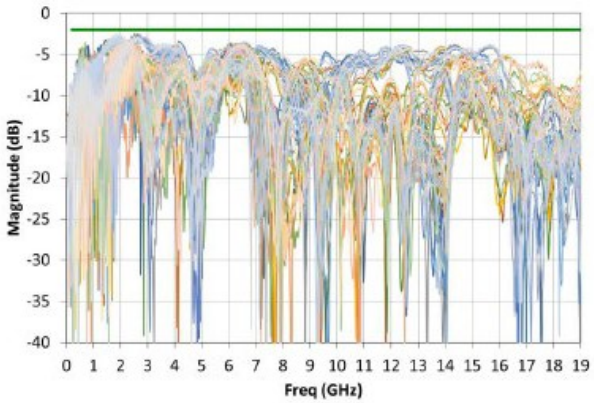
SCD22



SCC11

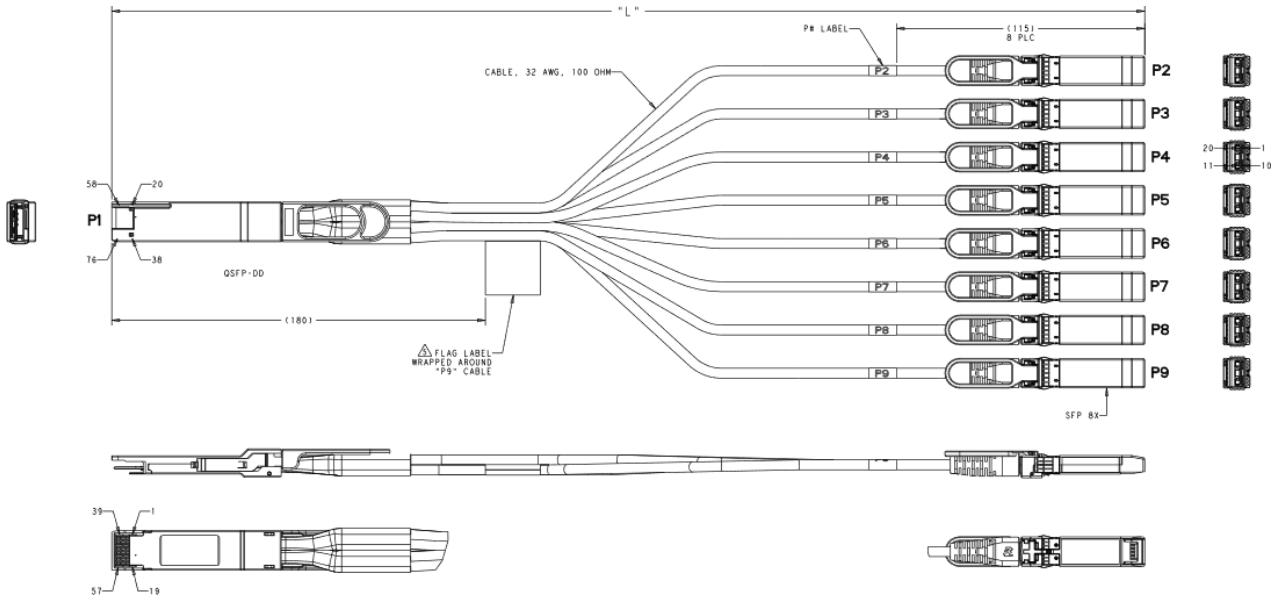


SCC22



Mechanical Specifications

QSFP-DD to 8xSFP 1m



About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is in engrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications from ranging from NEBS Level 3 to ISO 9001:2005 with every new development while maintaining the signature reliability of its products.

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