F5-UPG-QSFP28-LR4-AO

F5 Networks® F5-UPG-QSFP28 Compatible TAA 100GBase-LR4 QSFP28 Transceiver (SMF, 1295nm to 1309nm, 10km, LC, DOM)

Features

- SFF-8665 Compliance
- Duplex LC Connector
- Commercial Temperature 0 to 70 Celsius
- Single-mode Fiber
- Hot Pluggable
- Excellent ESD Protection
- Metal with Lower EMI
- RoHS Compliant and Lead Free



Applications

- 100GBase Ethernet
- Access and Enterprise

Product Description

This F5 Networks® F5-UPG-QSFP28 compatible QSFP28 transceiver provides 100GBase-LR4 throughput up to 10km over single-mode fiber (SMF) using a wavelength of 1295nm to 1309nm via an LC connector. It is guaranteed to be 100% compatible with the equivalent F5 Networks® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."

TAA COMPLIANT

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Maximum Supply Voltage	Vcc	-0.5		3.6	V
Storage Temperature	TS	-40		85	°C
Operating Case Temperature	Tc	0	25	70	°C
Operating Humidity	RH	5		85	%
Receiver Damage Threshold, per Lane	Rxdmg	5.5			dBm

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Dissipation	PD			3.5	W	
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Transmitter						
Differential data input swing per lane	Vin			900	Mvp-p	
Input Impedance (Differential)	Zin			10	%	
Stressed Input Parameters						
Eye width		0.46			UI	
Applied pk-pk sinusoidal jitter		IEEE 802.3bm Table 88-13				
Eye height		95			mv	
DC common mode voltage		-350		2850	mv	
Receiver						
Differential output amplitude		200		900	Mvp-p	
Output Impedance (Differential)	Zout			10	%	
Output Rise/Fall Time	tr/tf	12			ps	20%~80%
Eye width		0.57			UI	
Eye height differential		228			mv	
Vertical eye closure				5.5	db	

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Signaling Speed per Lane	Brave		25.78		Gbps	
Data Rate Variation		-100		+100		
Lane_0 Center Wavelength	λC0	1294.53	1295.56	1296.59	nm	
Lane_1 Center Wavelength	λC1	1299.02	1300.05	1301.09	nm	
Lane_2 Center Wavelength	λC2	1303.54	1304.58	1305.63	nm	
Lane_3 Center Wavelength	λC3	1308.09	1309.14	1310.19	nm	
Average Launch Power each Lane	P_{each}	-4.3		4.5	dBm	1
Optical Modulation Amplitude (OMA) each Lane	TxOMA	-1.3		4.5	dBm	
Difference in launch power between any two lanes (OMA)				5	dB	
Launch power in OMA minus TDP, each lane		-2.3			dBm	
Transmitter and dispersion penalty (TDP), each lane				2.2	dB	
Extinction Ratio	ER	4			dB	
Side-mode Suppression ratio	SMSRmin	30			dB	
Average launch power of OFF transmitter per lane				-30	dBm	
Relative Intensity Noise	RIN			-130	dB/hz	
Transmitter Reflectance				-12	dB	
Optical Return Loss Tolerance				20	dB	
Transmitter eye mask definitions: X1, X2, X3, Y1, Y2, Y3	0.25, 0.4, 0.45, 0.25, 0.28, 0.4					2
Receiver						
Signaling Speed per Lane	BRAVE		25.78		Gbps	
Data Rate Variation		-100		+100	ppm	
Damage threshold per lane	Rxdmg	5.5			dBm	
Lane_0 Center Wavelength	λC0	1294.53	1295.56	1296.59	nm	
Lane_1 Center Wavelength	λC1	1299.02	1300.05	1301.09	nm	
Lane_2 Center Wavelength	λC2	1303.54	1304.58	1305.63	nm	
Lane_3 Center Wavelength	λC3	1308.09	1309.14	1310.19	nm	
Average Receive Power per Lane	Rxpow	-10.6		4.5	dBm	3
Receive Power (OMA) per Lane	RxOMA			4.5	dBm	
Receive Sensitivity in OMA per Lane	Rxsens			-8.6	dBm	
Receiver 3 dB electrical upper cutoff frequency, per lane				31	GHz	
Stressed Receiver Sensitivity (OMA) per Lane	RXSRS			-6.8	dBm	4

Optical Return Loss	ORL			-26	dB	
LOS Assert	LOSA	-25			dBm	
LOS De-Assert	LOSD			-12	dBm	
LOS Hysteresis		0.5			dB	
Conditions of stressed receiver sensitivity test						
Vertical eye closure penalty	VECP	1.8			dB	5
Stressed eye J2 Jitter	J2	0.3			UI	5
Stressed eye J9 Jitter	J9	0.47			UI	5

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Hit ratio $5x10^{-5}$.
3. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
4. Measured with conformance test signal at TP3 for BER = 10–12.
5. Vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

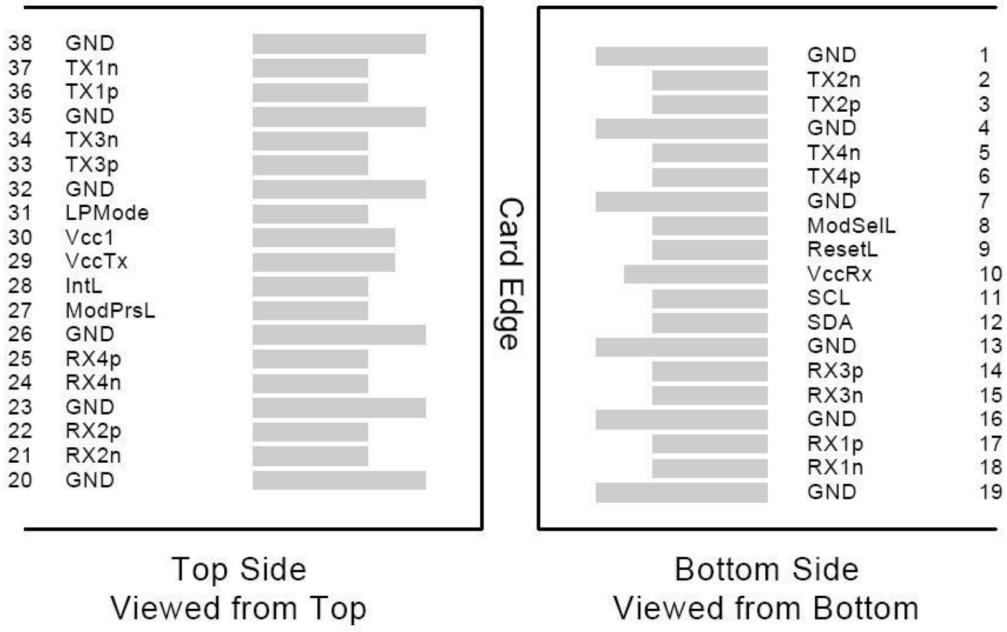
Pin Descriptions

Pin	Logic	Symbol	Name/Descriptions	Ref.
1		GND	Module Ground	1
2	CML-I	Tx2-	Transmitter inverted data input	
3	CML-I	Tx2+	Transmitter non-inverted data input	
4		GND	Module Ground	1
5	CML-I	Tx4-	Transmitter inverted data input	
6	CML-I	Tx4+	Transmitter non-inverted data input	
7		GND	Module Ground	1
8	LVTTL-I	MODSEIL	Module Select	2
9	LVTTL-I	ResetL	Module Reset	2
10		VCCRx	+3.3v Receiver Power Supply	
11	LVCMOS-I	SCL	2-wire Serial interface clock	2
12	LVCMOS-I/O	SDA	2-wire Serial interface data	2
13		GND	Module Ground	1
14	CML-O	RX3+	Receiver non-inverted data output	
15	CML-O	RX3-	Receiver inverted data output	
16		GND	Module Ground	1
17	CML-O	RX1+	Receiver non-inverted data output	
18	CML-O	RX1-	Receiver inverted data output	
19		GND	Module Ground	1
20		GND	Module Ground	1
21	CML-O	RX2-	Receiver inverted data output	
22	CML-O	RX2+	Receiver non-inverted data output	
23		GND	Module Ground	1
24	CML-O	RX4-	Receiver inverted data output	
25	CML-O	RX4+	Receiver non-inverted data output	
26		GND	Module Ground	1
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND	
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board	2
29		VCCTx	+3.3v Transmitter Power Supply	
30		VCC1	+3.3v Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	2
32		GND	Module Ground	1
33	CML-I	Tx3+	Transmitter non-inverted data input	
34	CML-I	Tx3-	Transmitter inverted data input	
35		GND	Module Ground	1
36	CML-I	Tx1+	Transmitter non-inverted data input	
37	CML-I	Tx1-	Transmitter inverted data input	
38		GND	Module Ground	1

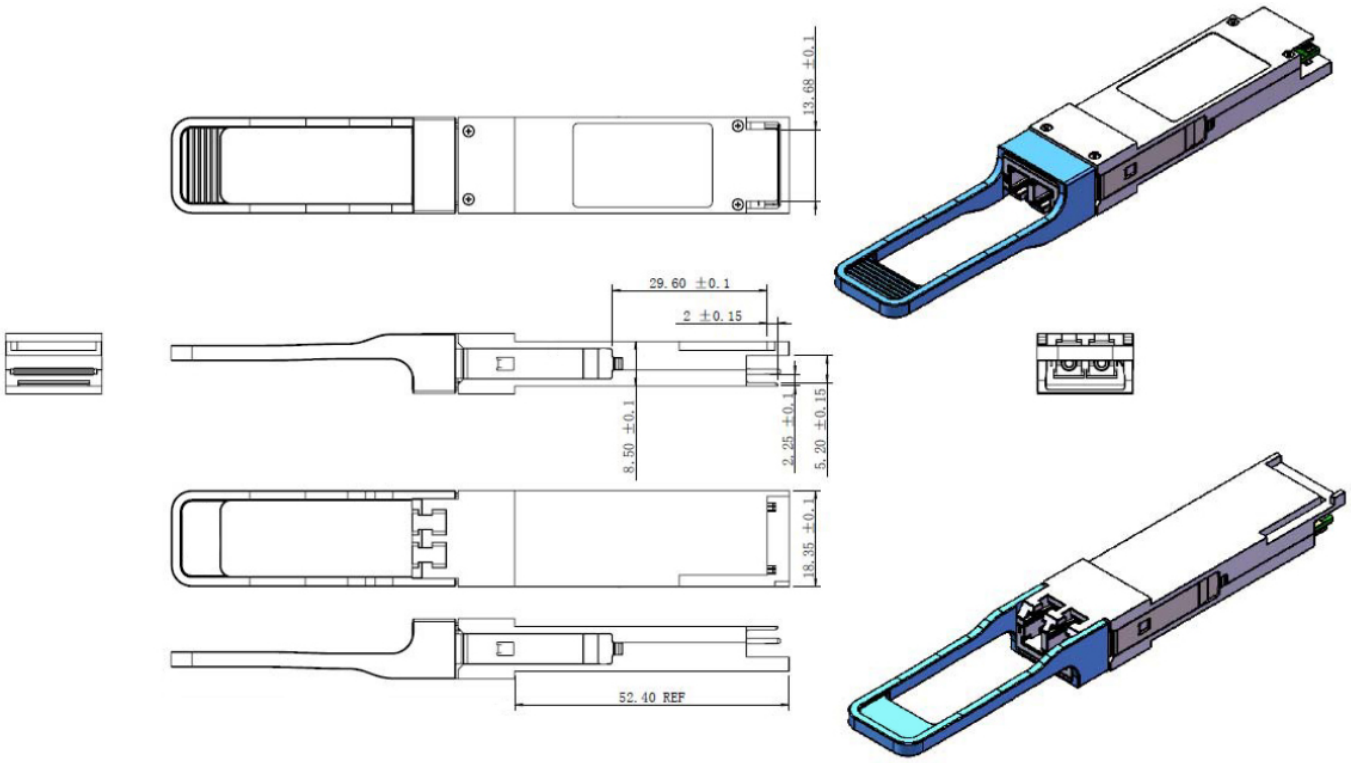
Notes:

1. Module circuit ground is isolated from module chassis ground with in the module.
2. Open collector; should be pulled up with 4.7k-10k ohms on host board to a voltage between 3.15V and 3.6V.

Electrical Pin-out Details



Mechanical Specifications



About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is in engrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications from ranging from NEBS Level 3 to ISO 9001:2005 with every new development while maintaining the signature reliability of its products.



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