Cisco Catalyst 9200 Series Switch Architecture

Contents

Introduction

Enterprise campus networks are undergoing profound changes to support ever-increasing bandwidth demands on the access layer, heightened by the introduction of 802.11ac and Wi-Fi 6 and the rapid growth of powerful endpoints requiring speeds from 10 Mbps to 10 Gbps. These networks are in dire need of an infrastructure that can scale rapidly and accommodate the new breed of endpoints without the need to replace the complete cabling infrastructure.

Cisco® Catalyst® 9200 Series Switches are the foundation of Cisco's next-generation enterprise-class access layer solutions. These fixed, stackable switches are sold in various configurations, including data, Power over Ethernet Plus (PoE+), and Multigigabit models. They deliver exceptional table scales (MAC/route/ACL) and buffering capabilities for enterprise applications. The Cisco Catalyst 9200 Series platform delivers up to 392 Gbps of switching capacity in standalone mode and 472 Gbps when stacked as eight-member switches, with up to 292 Million Packets Per Second (Mpps) of forwarding performance. The platform's stacking capability provides a flexible, pay-as-you-grow model as well as simplicity in the ability to manage multiple switches as a single logical switch. The switches provide two kinds of model types for different access layer requirements. C9200 models offer modular uplink options and FRU-able redundant power supplies. C9200L models offer fixed uplink options. Both provide non-blocking 1 Gigabit Ethernet and Multigigabit speeds (100 Mbps to 1, 2.5, 5, and 10 Gbps) over PoE+-capable copper ports. The two models offer uplink options that support nonblocking 40G Quad Small Form-Factor Pluggable (QSFP+) and 25G SFP28, 10G SFP+, and 1G SFP to meet diverse campus needs when connecting to aggregation or core devices.

This white paper provides an architectural overview of the Cisco Catalyst 9200 Series chassis, including system design, power, and cooling.

Platform overview

The Cisco Catalyst 9200 Series platform consists of fixed-configuration switches with airflow from the front and sides to the back. They are based on the Cisco Unified Access® Data Plane 2.0 mini (UADP) architecture, which not only protects your investment because of flexible and programmable pipelines but also allows a larger scale and higher throughput. The platform runs on the open Cisco IOS® XE Lite operating system, which supports model-driven programmability. Further, it supports all the foundational highavailability capabilities, including Cisco StackWise®-160 and StackWise-80 with stateful switchover, Platinum-efficient dual redundant power supplies, and variable-speed, high-efficiency, redundant fans.

Figure 1.
Cisco Catalyst 9200 Series Switches

The Cisco Catalyst 9200 Series includes the switches listed below, with variable port speeds and densities to meet the ever-increasing performance demands of enterprise campus environments and provide an architectural foundation for next-generation hardware features and scalability.

1G switches – C9200L fixed uplink models

Data-only switches (each with 1x UADP 2.0 mini ASIC)

C9200L-24T-4G: 24x 10M/100M/1G Ethernet ports with fixed 4x 1G uplink ports.

C9200L-48T-4G: 48x 10M/100M/1G Ethernet ports with fixed 4x 1G uplink ports.

C9200L-24T-4X: 24x 10M/100M/1G Ethernet ports with fixed 4x 10G uplink ports.

C9200L-48T-4X: 48x 10M/100M/1G Ethernet ports with fixed 4x 10G uplink ports.

PoE+ switches (each with 1x UADP 2.0 mini ASIC)

C9200L-24P-4G: 24x 10M/100M/1G Ethernet ports with fixed 4x 1G uplink ports – a maximum PoE budget of 740W.

C9200L-48P-4G: 48x 10M/100M/1G Ethernet ports, with fixed 4x 1G uplink ports – a maximum PoE budget of 1440W.

C9200L-24P-4X: 24x 10M/100M/1G Ethernet ports with fixed 4x 10G uplink ports – a maximum PoE budget of 740W.

C9200L-48P-4X: 48x 10M/100M/1G Ethernet ports with fixed 4x 10G uplink ports – a maximum PoE budget of1440W.

Partial PoE+ switches(each with 1x UADP 2.0 mini ASIC)

C9200L-48PL-4G: 48x 10M/100M/1G Ethernet ports with fixed 4x 1G uplink ports – a maximum PoE budget of 370W.

C9200L-48PL-4X: 48x 10M/100M/1G Ethernet ports with fixed 4x 10G uplink ports – a maximum PoE budget of 370W.

Multigigabit Ethernet switches with PoE+ (each with 2x UADP 2.0 mini ASIC)

C9200L-24PXG-4X: 8x 100M/1G/2.5G/5G/10G and 16x 10M/100M/1G Ethernet copper ports with fixed 4x 10G uplink ports – maximum PoE budget of 740W.

C9200L-48PXG-4X: 12x 100M/1G/2.5G/5G/10G and 36x 10M/100M/1G Ethernet copper ports with fixed 4x 10G uplink ports – maximum PoE budget of 1440W.

C9200L-24PXG-2Y: 8x 100M/1G/2.5G/5G/10G and 16x 10M/100M/1G Ethernet copper ports with fixed 2x 25G uplink ports – maximum PoE budget of 740W.

C9200L-48PXG-2Y: 8x 100M/1G/2.5G/5G/10G and 40x 10M/100M/1G Ethernet copper ports with fixed 2x 25G uplink ports – maximum PoE budget of 1440W.

1G switches – C9200 modular uplink models

Data-only switches
(each with 1x UADP 2.0 mini ASIC)

C9200-24T: 24x 10M/100M/1G Ethernet ports with optional uplink modules.

C9200-48T: 48x 10M/100M/1G Ethernet ports with optional uplink modules.

PoE+ switches
(each with 1x UADP 2.0 mini ASIC)

C9200-24P: 24x 10M/100M/1G Ethernet ports with optional uplink modules - maximum PoE budget of 740W.

C9200-48P: 48x 10M/100M/1G Ethernet ports with optional uplink modules - maximum PoE budget of 1440W.

C9200-24PB: 24x 10M/100M/1G Ethernet ports, enhanced VRF, with optional uplink modules - maximum PoE budget of 740W.

C9200-48PB: 48x 10M/100M/1G Ethernet ports, enhanced VRF, with optional uplink modules - maximum PoE budget of 1440W.

Partial PoE+ switches(each with 1x UADP 2.0 mini ASIC)

C9200-48PL: 48x 10M/100M/1G Ethernet ports with optional uplink modules - maximum PoE budget of 370W.

Multigigabit Ethernet switches with PoE+
(each with 2x UADP 2.0 mini ASIC)

C9200-24PXG: 8x 100M/1G/2.5G/5G/10G and 16x 10M/100M/1G Ethernet copper ports with optional uplink modular - maximum PoE budget of 740W.

C9200L-48PXG-4X: 8x 100M/1G/2.5G/5G/10G and 40x 10M/100M/1G Ethernet copper ports with optional uplink modular - maximum PoE budget of 1440W.x

Switch overview

Chassis design

This section briefly covers the high-level system design of the Cisco Catalyst 9200 Series. It is a very simple and flexible architecture, with the option to combine up to eight physical switches as one logical switch using Cisco StackWise-160 technology for modular SKUs and StackWise-80 technology for fixed SKUs.

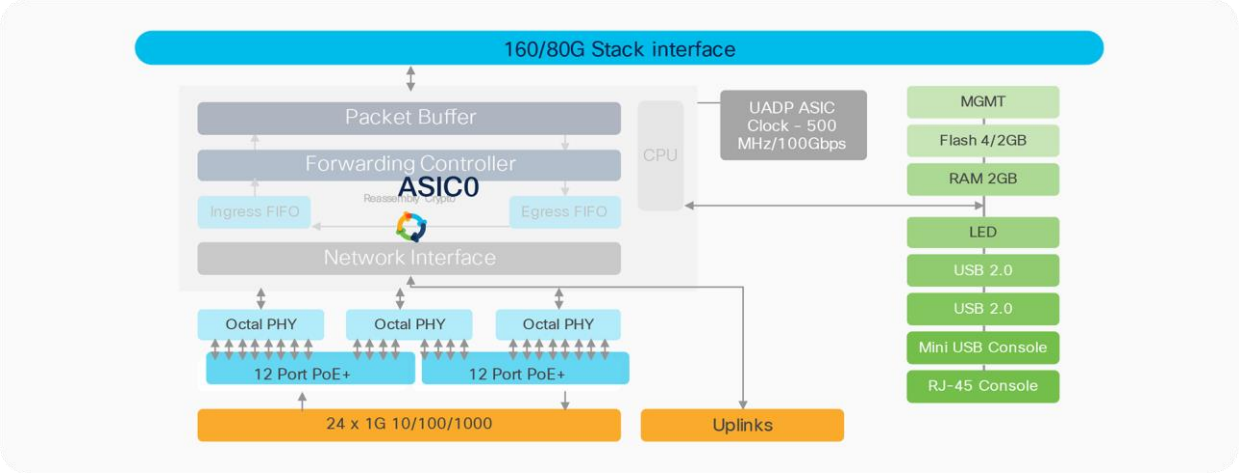

Figure 2.
C9200-24P board layout

Cisco Catalyst 9200 Series switches come with two field-replaceable Power Supply Unit (PSU) slots and support AC power inputs. There are two redundant variable-speed fans in the back of the switch. All Catalyst 9200 Series models come with a built-in passive RFID for inventory management, a Blue Beacon LED for device-level identification, and a tricolor LED for system status.

These switches also include two StackWise-160 (for C9200 modular SKUs) and two StackWise-80 (for C9200L fixed SKUs) ports, an RJ-45 console port, and a 1G management port. The front of the switch has a USB Type B connector for connecting a console to the switch and two USB 2.0 slots.

Chassis power

Cisco Catalyst 9200 Series switches support up to two 125W, 600W, or 1000W AC PSUs. The 600W and 1000W PSUs are rated as Platinum efficient for greater than 90 percent power efficiency at 100 percent load. The 125W PSU is rated as Silver efficient for greater than 80 percent power efficiency at 100 percent load. The system supports either one PSU operating in standalone mode, which is sufficient to power the switch in its maximum configuration, or two PSUs operating in redundant load-sharing mode for PoE+ SKUs. In the data-only SKUs, the system supports either one PSU operating in standalone mode or two PSUs operating in redundant mode.

Figure 3.
Power supply slot

Power supply unit

The maximum output power per power supply for the Cisco Catalyst 9200 Series is listed below. Each PSU has a power holdup time of approximately 20 milliseconds at 100 percent load. Each comes with front-to-back variable speed cooling fans and has a push-release lock for simple and secure Online Insertion and Removal (OIR).

- The 1000W AC PSU has maximum output of 1000W at 110V to 220V input.
- The 600W AC PSU has maximum output of 600W at 110V to 220V input.
- The 125W AC PSU has maximum output of 125W at 110V to 220V input.

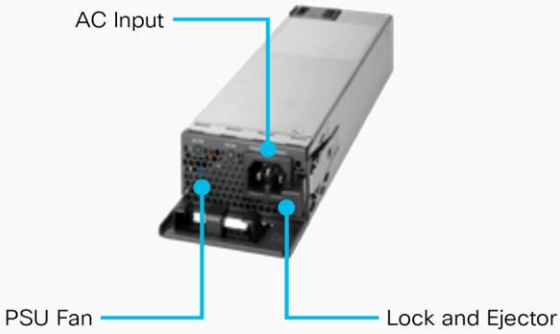

Figure 4.
Power supply unit

Each PSU supports a bicolor (green/red) LED to show the status of the power supply.

Table 1. Meaning of AC PSU LED

LED	Color	Status	Description
AC	●	Off	No AC input power
AC	●	On	AC input power present
PS	●	Off	Output is disabled
PS	●	On	Power Output to switch active
PS	●	Fail	Output has failed

Chassis cooling

Cisco Catalyst 9200 Series switches support hot-swappable and field-replaceable fans (for the C9200 modular SKUs) and fixed fans (for the C9200L fixed SKUs) in the rear of the chassis. They are variable-speed fans supporting airflow from front to back. The fan unit is responsible for cooling the entire chassis and interfacing with environmental monitors to trigger alarms when conditions exceed thresholds. The fan modules contain thermal sensors to detect ambient temperature and adjust the fan speed. The chassis supports a hardware failure of up to one individual fan; the remaining fans will automatically increase their speed to compensate and maintain sufficient cooling. If the switch fails to meet the minimum number of required fans, the switch shuts down automatically to keep the system from overheating.

Cisco Catalyst 9200 Series chassis are equipped with onboard thermal sensors to monitor the ambient temperature at various points and report thermal events to the system so that it can adjust the fan speed.

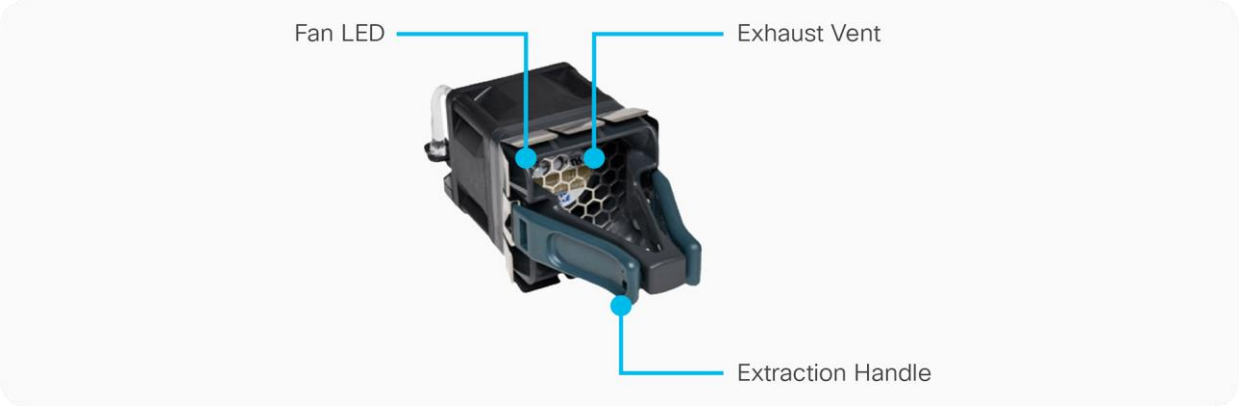

Figure 5.
Fan module for C9200 modular SKUs

Insertion and removal of the fan modules is made easy with fan assembly levers and ejectors. To remove the module, press the fan ejector lever and use the fan handle.

Table 2. Meaning of fan LED

LED	Color	Status	Description
FAN		Solid	Fan/Fans OK
FAN		Solid	Tachometer fault
FAN		Solid	One or more fans faulty (tachometer) Exceeded maximum limit

Chassis airflow

The Cisco Catalyst 9200 Series fan supports airflow from the front and sides to the back.

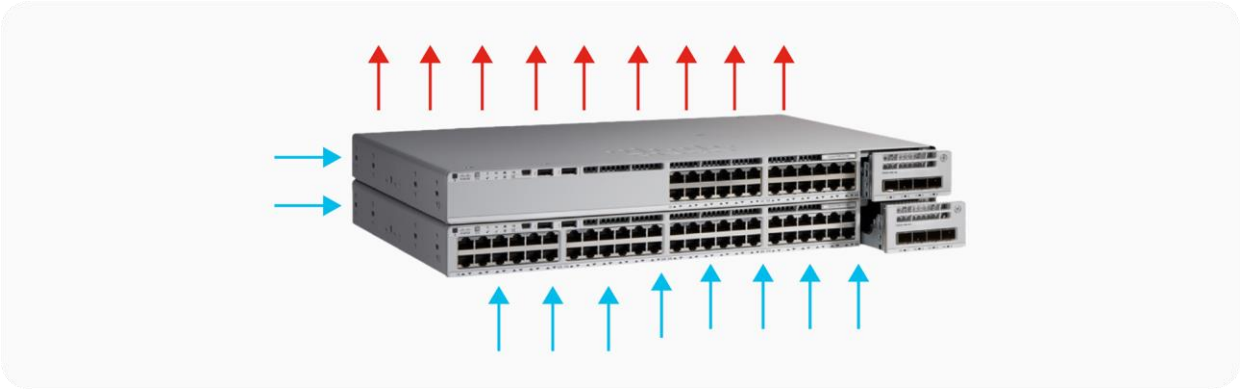

Figure 6.
Airflow

The switch supports port-side and side intake airflow on all Catalyst 9200 Series models, in which air enters the switch through the sides and ports (cold aisle) and exhausts through the fan and power supply modules in the rear (hot aisle).

Baseboard components

Cisco Catalyst 9200 Series switches are line-rate switches that offer configurable system resources to optimize support for specific features, depending on how the switch is used in the network. The switch architecture consists of five main components:

- UADP Application-Specific Integrated Circuit (ASIC)
- Embedded CPU
- ASIC interconnect
- StackWise-160 or StackWise-80
- Front-panel interfaces

UADP ASIC

The Cisco Catalyst 9200 Series is built with the UADP 2.0 mini ASIC, which is based on System-On-Chip (SOC) architecture. UADP 2.0 is the third generation of the UADP family. It uses 28-nanometer technology and a single core capable of switching 100 GB of data at line rate, and is specifically optimized for next-generation fixed access switches.

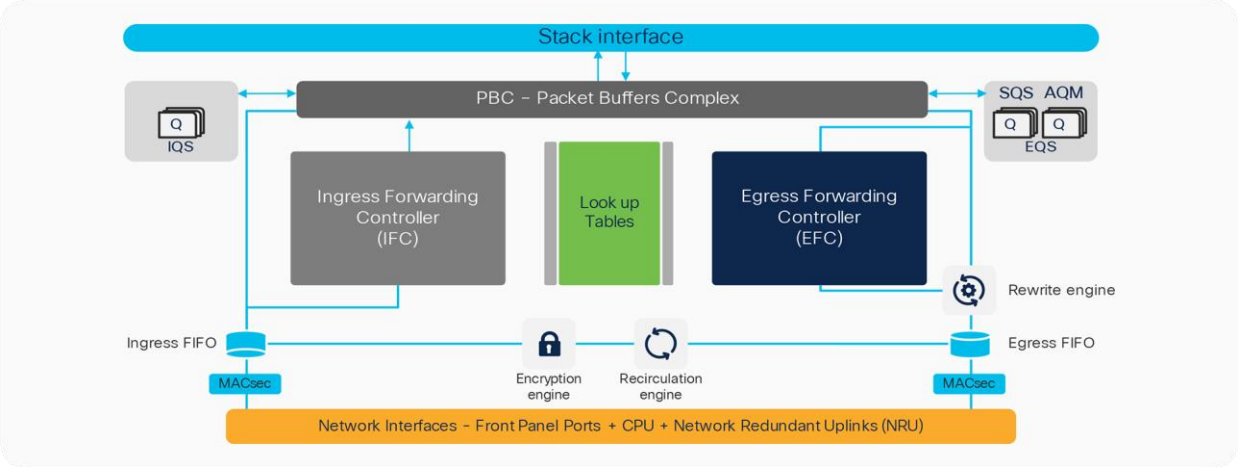

Figure 7.
UADP 2.0 ASIC block diagram

The architecture and functionality of UADP 2.0 are largely unchanged from previous generations. The key UADP 2.0 capabilities are as follows:

- Packet bandwidth and switching throughput: 100G
- Forwarding performance: 291 Mpps
- Stack bandwidth: 160 Gbps
- Packet buffer: 6 MB
- Dedicated NetFlow block with 16,000/8,000 IPv4/v6

Embedded CPU complex

Cisco Catalyst 9200 Series switches are equipped with an embedded CPU on the ASIC.

Highlights include:

- 4-core 1.4-GHz embedded ARM
- Single 4 GB of DDR3 RAM
- Flash on RAM: 4 GB
- Support for USB Type B file system (front serviceable) for external storage and Bluetooth dongle
- Support for USB Type B serial console in addition to the RJ-45 serial console
- System reset switch for manual power cycle

ASIC interconnect or internal stack interface

Cisco Catalyst 9200 Series switches come with either a single ASIC or dual ASICs, as explained later. The models with dual ASICs leverage the internal stack interface to transport traffic between the front-panel ports of different ASICs.

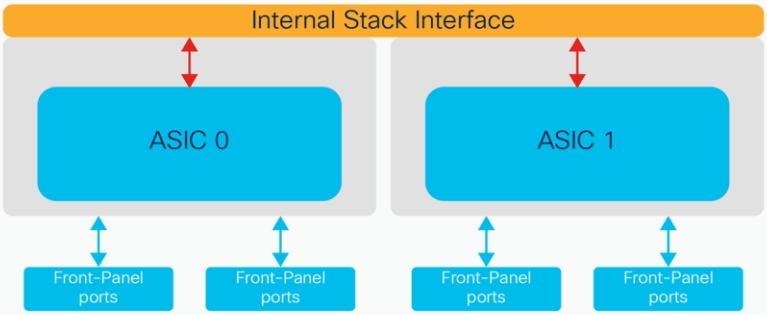

Figure 8.
Dual-ASIC diagram

The stack interface is capable of switching 80 Gbps between the ASICs. Internally this stack interface consists of two rings, each capable of 40 Gbps, providing a cumulative bandwidth of 160 Gbps (80 Gbps in full duplex) dedicated to switching traffic between the ASICs.

Stack interface features include:

- No packet size limitations
- Packet type agnostic
- Packet data is spread across all the rings
- Header compression capabilities
- No buffering on stack interface

StackWise-160

The Cisco Catalyst 9200 Series provides the ability to combine multiple switches into one logical switch when connected together using special cables on StackWise-160 ports on the back. Up to eight switches can be connected in the stack, delivering operational simplicity and higher port density with combined switching capacity and maximum resiliency.

Figure 9.
Switches stacked using StackWise-160

Stacking in the Cisco Catalyst 9200 Series is enabled using a stack-ring fabric known as StackWise-160. The "160" in the name refers to the total available stack capacity: 160 Gbps. The fabric consists of two counter-rotating rings (40 Gbps per ring), and the system's throughput is a function of the aggregated throughput of these rings (80 Gbps). A technique called spatial reuse doubles throughput on the stack's rings. Spatial reuse is enabled by destination-based packet stripping and also by allowing multiple flows to coexist. Spatial reuse frees available bandwidth on the ring, as the destination switch strips packets destined to itself, allowing other stack members to insert additional packets onto the ring.

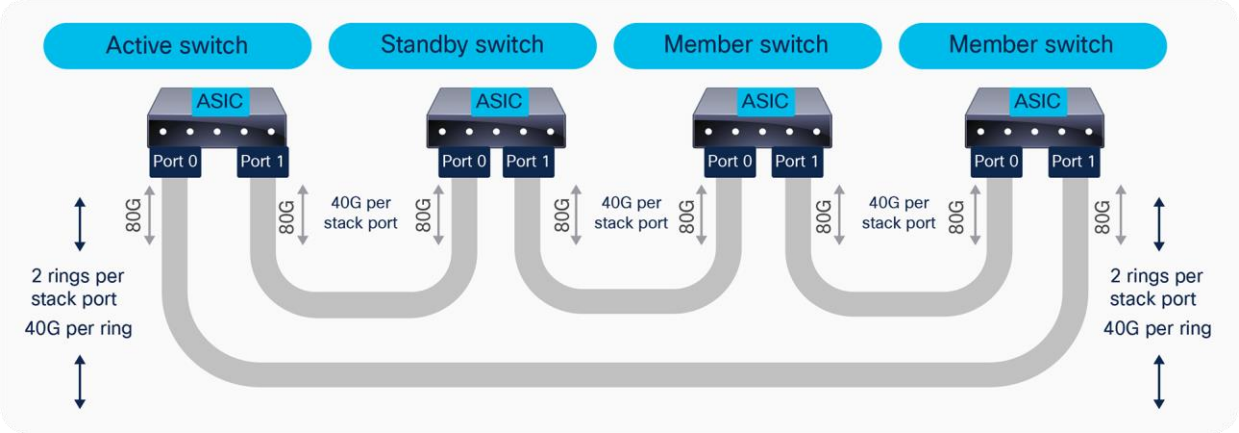

Figure 10.
StackWise-160 architecture

Stackwise-160 creates a unified control and management plane by electing one switch in the stack as an active switch and another switch as a hot standby. The remaining switches become stack members. The active switch is responsible for all Layer 2 and Layer 3 network control processing and for synchronizing all state information with the hot standby. The active switch unifies management for the entire stack, performing configuration and monitoring for the stack.

The forwarding architecture is designed to provide distributed switching across all member switches in the stack.

Each switch in the stack optimizes data plane performance by using its local hardware resources.

StackWise-160 highlights

- All C9200 modular models are supported in the stack
- No packet size limitations
- Packet type agnostic
- No buffering on stack interface
- Packet data is spread across all the rings

StackWise-80

Stackwise-80 is completely identical in architecture to Stackwise-160, except that it has half the capacity, with a stacking bandwidth of 80 Gbps. The C9200L fixed SKUs support the Stackwise-80 architecture.

Note: The fixed C9200L switches and the modular C9200 switches cannot be stacked together.

Front-panel interfaces

Ethernet PHY (physical layer) connects a link layer device (often a MAC) to a physical medium such as a transceiver. PHY on Cisco Catalyst 9200 Series switches is a fully integrated Ethernet transceiver that supports steering and mapping of lanes back to the ASIC to support multiple speeds (1G, 10G), depending on the optics inserted on the front-panel ports.

Highlights of the C9200L-24T-4X, C9200L-24T-4G, C9200L-24P-4X, C9200L-24P-4G, C9200-24T, and C9200-24P models are as follows:

- 24x 1G RJ-45 Ethernet ports, all mapped to the single core on a single ASIC.
- All of the uplink ports connect to ASIC0/Core0.
- Port mapping:
  - All of the ports—1 through 24—are mapped to ASIC0/Core0.

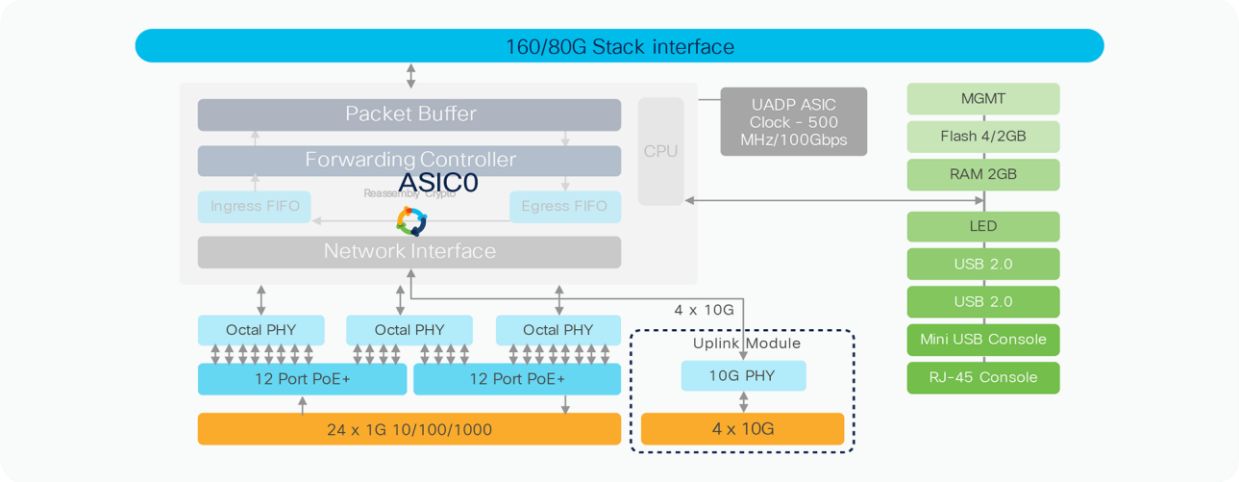

Figure 11.
C9200L-24P-4X high-level block diagram

Highlights of the C9200L-48T-4X, C9200L-48T-4G, C9200L-48P-4X, C9200L-48P-4G, C9200-48T, and C9200-48P models are as follows:

- 48x 1G RJ-45 Ethernet ports all mapped to the single core on a single ASIC.
- All of the uplink ports connect to ASIC0/Core0.
- Port mapping:
  - All of the ports—1 through 48—are mapped to ASIC0/Core0.

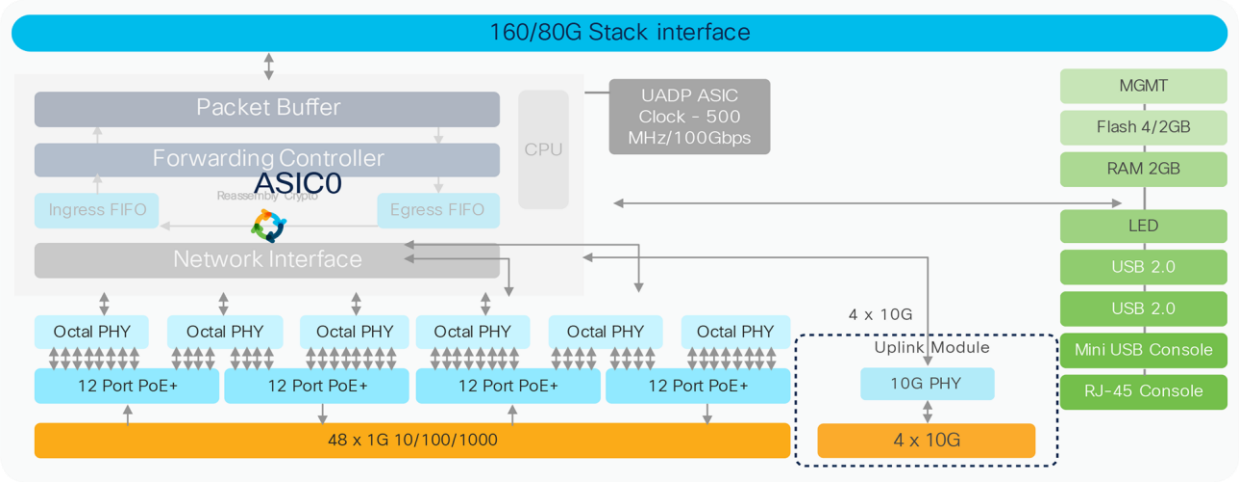

Figure 12.
C9200L-48P-4X high-level block diagram

Highlights of the C9200-24PXG and C9200L-24PXG-4X models are as follows:

- These models provides 8x 1G, 2.5G, 5G, or 10G RJ-45 Ethernet ports (for 10G, use Category 6a or above) and 16x 1G RJ-45 Ethernet ports.
- These models also offers PoE+ inline power on all ports.
- Uplink ports are split between ASIC0/Core0 and ASIC1/Core0.
- Port mapping:
  - Ports 1 through 16 are mapped to ASIC1/Core0.
  - Ports 17 and 18 are mapped to ASIC1/Core0.
  - Ports 19 through 24 are mapped to ASIC0/Core0.

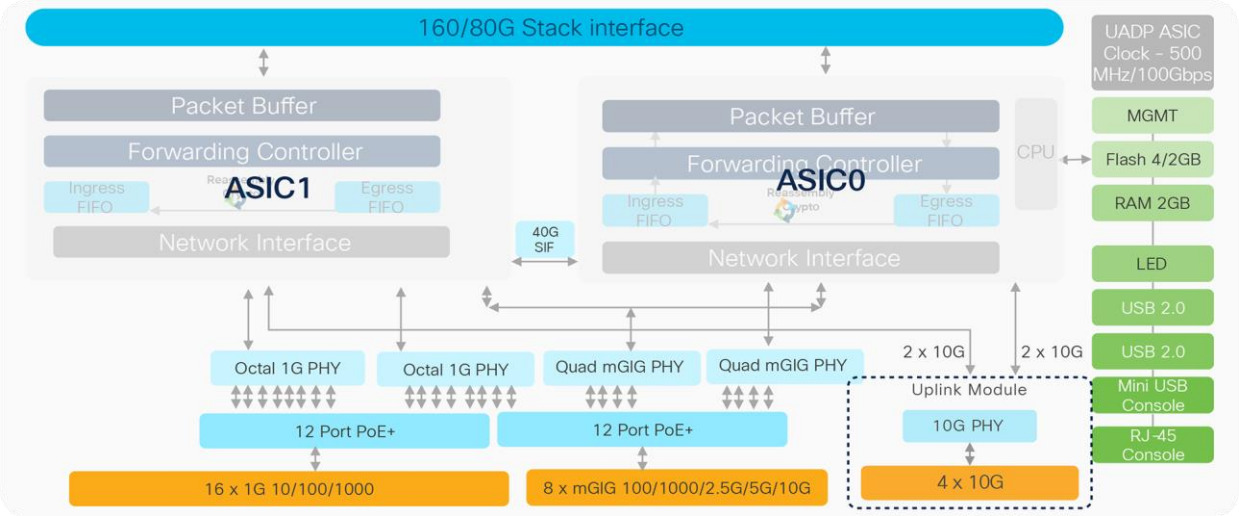

Figure 13.
C9200L-24PXG-4X high-level block diagram

Highlights of the C9200L-48PXG-4X model are as follows:

- This model provides 12x 1G, 2.5G, 5G, or 10G RJ-45 Ethernet ports (for 10G, use Category 6a or above) and 36x 1G RJ-45 Ethernet ports.
- This model also offers PoE+ inline power on all ports.
- Of the four 10G uplink ports, two connect to ASIC0/Core0 and the other two connect to ASIC1/Core0.
- Port mapping:
  - Ports 1 through 36 are mapped to ASIC1/Core0.
  - Ports 37 through 40 are mapped to ASIC1/Core0.
  - Ports 41 through 48 are mapped to ASIC0/Core0.

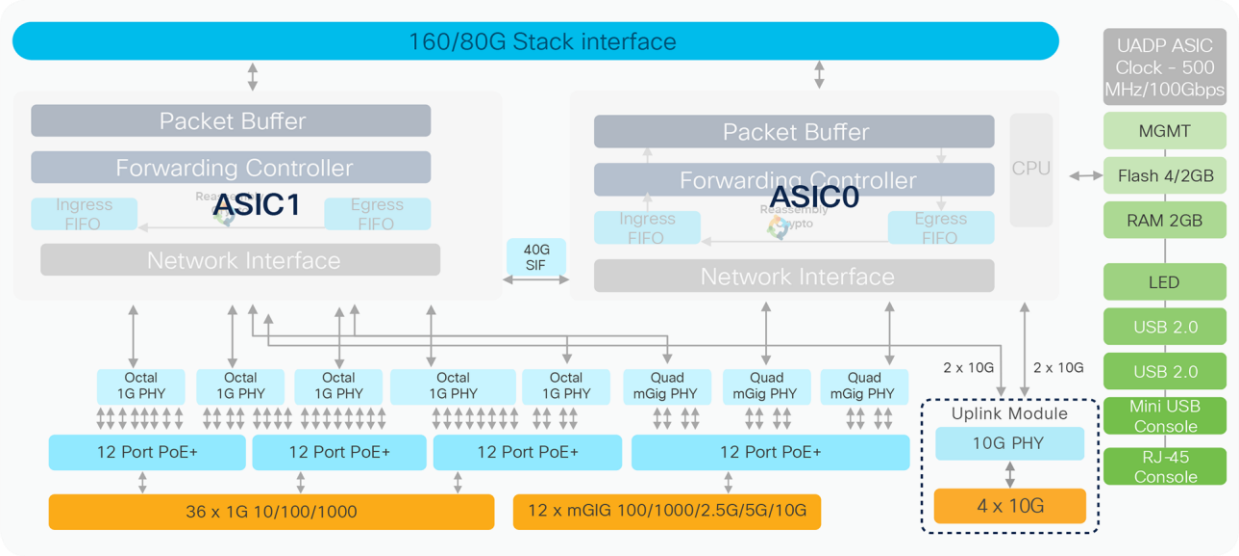

Figure 14.
C9200L-48PXG-4X high-level block diagram

Highlights of the C9200-48PXG and C9200L-48PXG-2Y models are as follows:

- These models provides 8x 1G, 2.5G, 5G, or 10G RJ-45 Ethernet ports (for 10G, use Category 6a or 7 cables) and 40x 1G RJ-45 Ethernet ports.
- These models also offers PoE+ inline power on all ports.
- Uplink ports are split between ASIC0/Core0 and ASIC1/Core0.
- Port mapping:
  - Ports 1 through 40 are mapped to ASIC1/Core0.
  - Ports 41 and 42 are mapped to ASIC1/Core0.
  - Ports 43 through 48 are mapped to ASIC0/Core0.

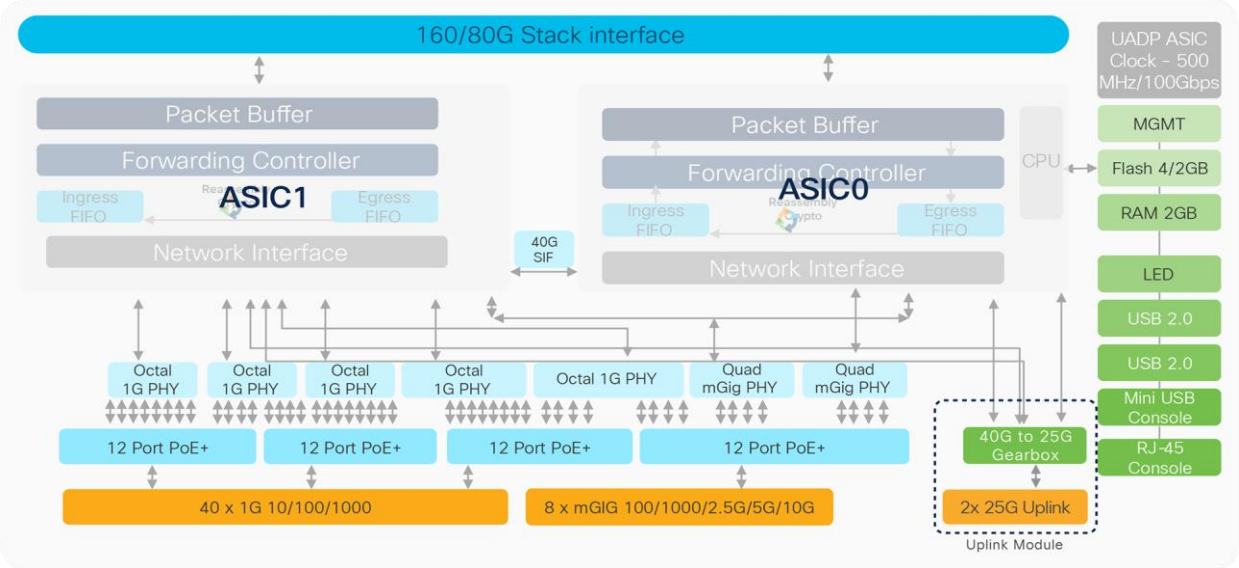

Figure 15.
C9200L-48PXG-2Y high-level block diagram

Highlights of the C9200-24PXG, C9200L-24PXG-2Y model are as follows:

- These models provides 8x 1G, 2.5G, 5G, or 10G RJ-45 Ethernet ports (for 10G, use Category 6a or above) and 16x 1G RJ-45 Ethernet ports.
- These models also offers PoE+ inline power on all ports.
- Uplink ports are split between ASIC0/Core0 and ASIC1/Core0.
- Port mapping:
  - Ports 1 through 16 are mapped to ASIC1/Core0.
  - Ports 17 and 18 are mapped to ASIC1/Core0.
  - Ports 19 through 24 are mapped to ASIC0/Core0.

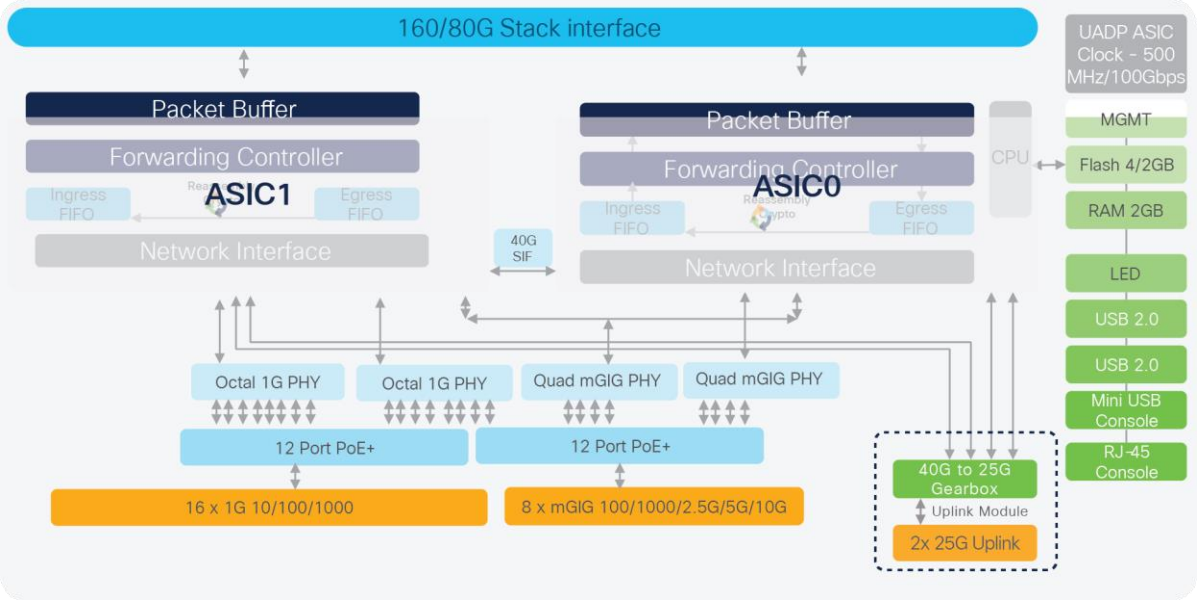

Figure 16.
C9200L-24PXG-2Y high-level block diagram

Network modules

The Cisco Catalyst 9200 Series modular SKUs (C9200) support four optional network modules for uplink ports on all models. The default switch configuration does not include the network modules. All ports on the network module are line rate, and all software features supported on the switch downlink ports are also supported on the network module ports.

Figure 17.
Network modules

Highlights of the network modules are as follows:

- Uplink modules are supported on Catalyst 9200 Series modular models (C9200).
- Modules are automatically powered upon insertion.
- Modules are OIR capable.
- Modules are ACT2 authenticated.
- Line rate on every port, with 10G single-flow traffic processing.
- Speed is auto-negotiated depending on the optics inserted.

Packet walks

This section provides a high-level overview of how packet forwarding is performed on Cisco Catalyst 9200 Series switches. Since the UADP ASICs used on all Catalyst 9200 Series models are architecturally equivalent, single unicast packet walks are described.

Ingress and egress unicast forwarding within ASIC

The figure below illustrates unicast packet forwarding within the ASIC.

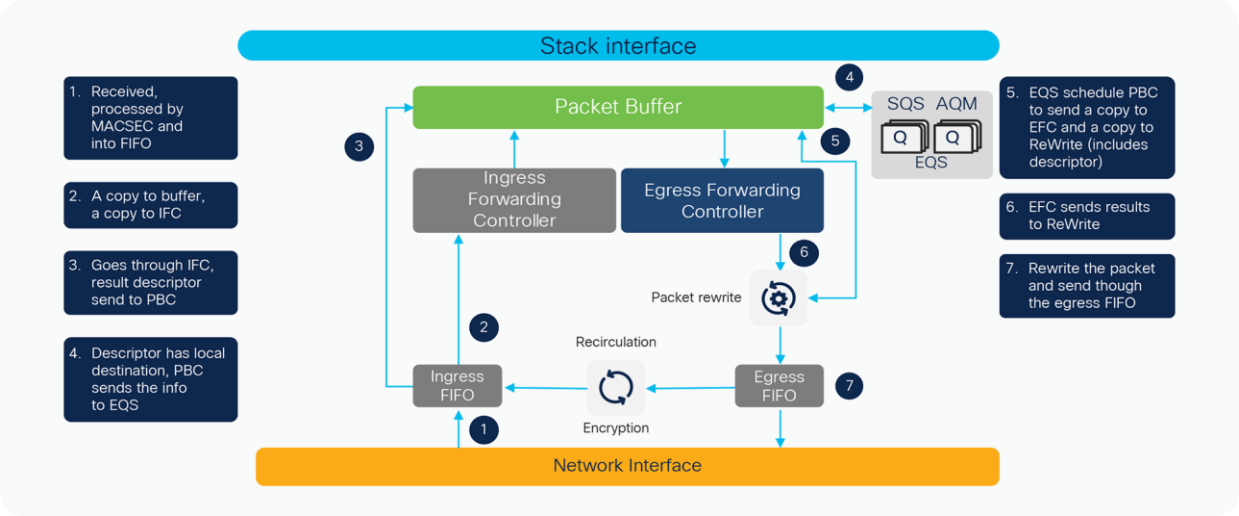

Figure 18.
Packet walk within ASIC

The following is the basic sequence of events when packets enter the Cisco Catalyst 9200 Series front-panel ports:

1. Packet arrives at ingress port. PHY converts the signal and serializes the bits, and then sends the packet to the NIF (Network Interface) on the ASIC.
2. NIF packages frame into 256-byte chunks and moves them to the ingress MACsec engine. NIF also implements 1588 timestamping and Energy Efficient Ethernet (EEE) if enabled.
3. MACsec engine is a cut-through, fixed-latency cryptography engine to support 802.1AE MAC Security. Core cryptography of Layer 2 Cisco TrustSec® and output frames go to ingress FIFO.
4. Ingress FIFO collects the frames in 256-byte segments and transmits them to the unified Packet Buffer Complex (PBC).
5. Ingress Forwarding Controller (IFC) snoops packets between ingress FIFO and PBC and performs frame processing and a series of table lookups to deliver the resulting frame descriptor to PBC.
6. PBC is the primary packet store on the UADP ASIC. It uses the 64-byte frame descriptor to determine the egress port and QoS treatment of the frame. As the egress port is on the same ASIC, PBC performs local switching by allowing frames to be enqueued directly into egress queues.
7. EQS (Egress Queues and Scheduler) is responsible for queue management, replication, and scheduling packets. EQS enqueues packets arriving from the local ingress path into egress queue structures and then schedules them for transmission to the corresponding egress ports.

8. PBC receives the packet handle/results from the EQS block and sends the packet to the egress FIFO through the rewrite engine.
9. EFC (egress forwarding controller) snoops the frames as they move from PBC to the rewrite engine.
10. EFC completes egress lookup functions (such as egress switched port analyzer [SPAN] and recirculation) and writes the rewrite descriptor to the rewrite engine.
11. Rewrite engine performs packet rewrite with new descriptor and fragmentation. Packets are rewritten first and then fragmented if necessary and sent to the egress port FIFO. The egress port FIFO provides storage for frames awaiting transmission to either the NIF or the recirculation path.
12. Egress MACsec performs fixed-latency and wire-rate encryption required by the frame for 802.1AE or Layer 2 Cisco TrustSec and then passes the frame on to the NIF in a cut-through manner.

Ingress and egress unicast forwarding across ASICs

The figure below illustrates unicast packet forwarding across ASICs.

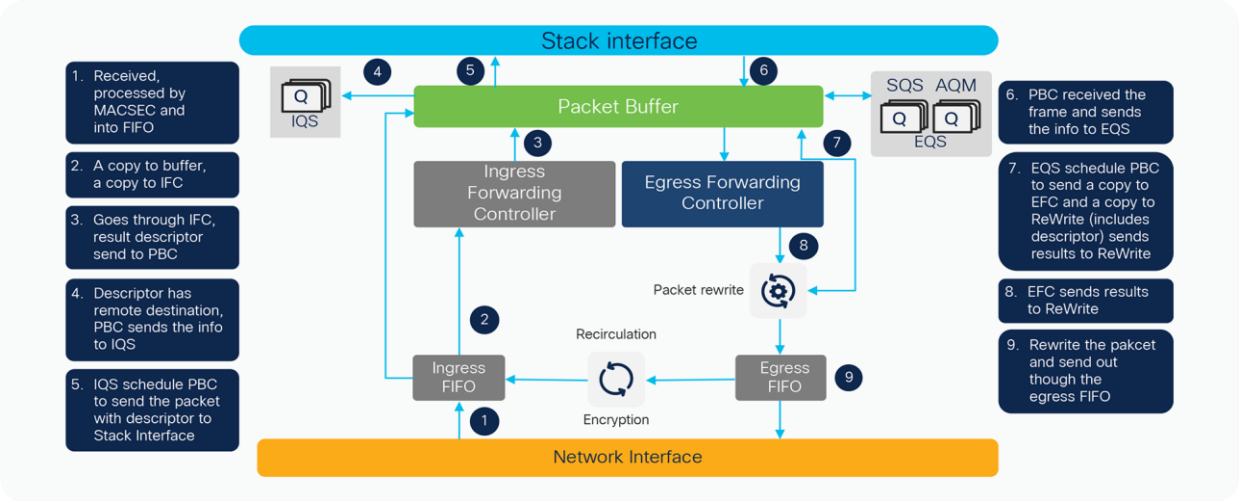

Figure 19.
Packet walk across ASICs

The following is the basic sequence of events when packets enter the Cisco Catalyst 9200 Series front-panel ports:

1. Packet arrives at ingress port. PHY converts the signal and serializes the bits, and then sends the packet to the NIF (Network Interface) on the ASIC.
2. NIF packages frame into 256-byte chunks and moves them to the ingress MACsec engine. NIF also implements 1588 timestamping and EEE if enabled.
3. MACsec engine is a cut-through, fixed-latency cryptography engine to support 802.1AE MAC Security. Core cryptography of Layer 2 Cisco TrustSec and output frames go to ingress FIFO.
4. Ingress FIFO collects the frames in 256-byte segments and transmits them to the unified Packet Buffer Complex (PBC).
5. Ingress Forwarding Controller (IFC) snoops packets between ingress FIFO and PBC and performs frame processing and a series of table lookups to deliver the resulting frame descriptor to PBC.

6. PBC is the primary packet store on the UADP ASIC. It uses the 64-byte frame descriptor to determine the egress port and QoS treatment of the frame. As the egress port is on a remote UADP ASIC, PBC sends the frame descriptor to the Ingress Queue and Scheduler (IQS).
7. IQS provides queueing and scheduling functions along with congestion management (priority packets are enqueued first on the stack interface) before sending packet to remote UADP ASICs.
8. IQS notifies PBC to dequeue a frame from the stack interface once the queues are available for transmission.
9. Packets arriving from the stack interface are buffered in PBC and a descriptor is sent to EQS for further processing.
10. EQS (Egress queues and scheduler) is responsible for queue management, replication, and scheduling packets. EQS enqueues packets arriving from the local ingress path into egress queue structures and then schedules them for transmission to the corresponding egress ports.
11. PBC receives the packet handle/results from the EQS block and sends the packet to egress FIFO through the rewrite engine.
12. EFC (egress forwarding controller) snoops the frames as they move from PBC to the rewrite engine.
13. EFC completes egress lookup functions (such as egress SPAN and recirculation) and writes the rewrite descriptor to the rewrite engine.
14. Rewrite engine performs packet rewrite with new descriptor and fragmentation. Packets are rewritten first and then fragmented if necessary and sent to the egress port FIFO. The egress port FIFO provides storage for frames awaiting transmission to either the NIF or recirculation path.
15. Egress MACsec performs fixed-latency and wire-rate encryption required by the frame for 802.1AE or Layer 2 Cisco TrustSec and then passes the frame on to the NIF in a cut-through manner.

Conclusion

Cisco Catalyst 9200 Series Switches are the enterprise-class access switches in the Cisco Catalyst 9000 family, offering a comprehensive portfolio and architectural flexibility with 1- and 10-Gbps downlink ports and 10- and 25-Gbps uplink ports. This new platform is based on Cisco's next-generation programmable UADP ASIC for increased bandwidth, scale, security, and telemetry. The Cisco Catalyst 9200 Series is built on a flexible stacking architecture designed to provide high performance to meet the evolving needs of highly scalable and growing enterprise networks.

References

Additional websites that offer more details about the Cisco Catalyst 9200 Series and its capabilities:

Cisco Catalyst 9200 Series Switches Data Sheet

Cisco Catalyst 9200 Series Switches Hardware Installation Guide

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